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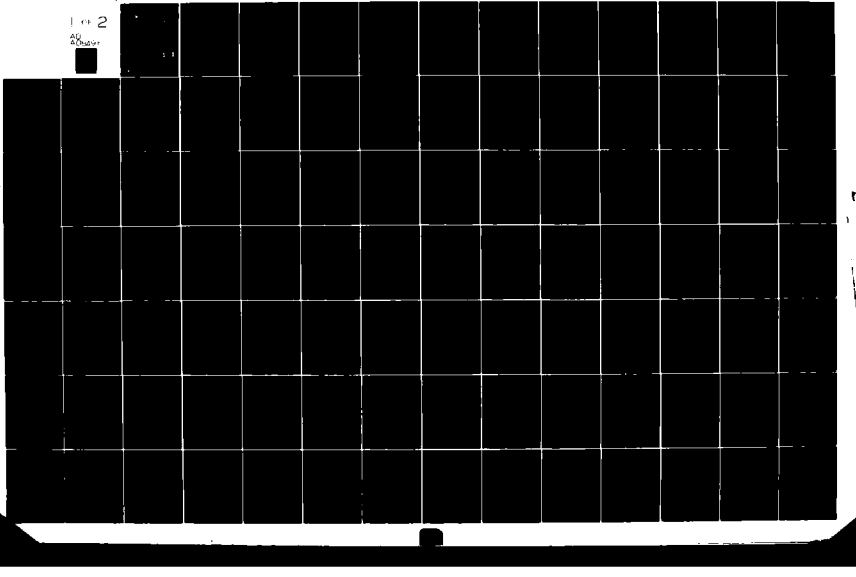
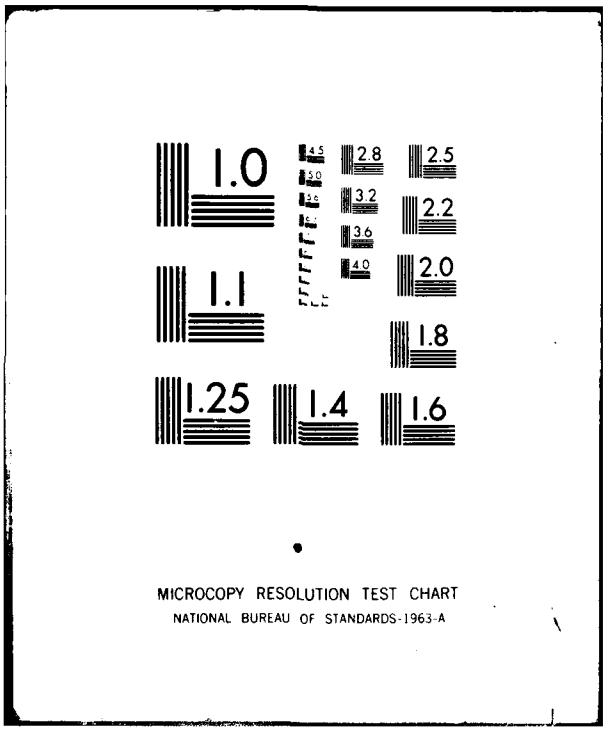
INTEGRATED CIRCUIT TESTER EVALUATION STUDY.(U)
MAR 80 P STEVENS
UNCLASSIFIED NAEC-MISC-82-0380 6IDEP -E150-0500 NL

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26 APR 1979

NAVAL AIR ENGINEERING CENTER
LAKEHURST, N.J.
08733

NAEC-MISC-92-0380

LEVEL II

INTEGRATED CIRCUIT TESTER

EVALUATION STUDY

Avionics Support Equipment Division
Ground Support Equipment Department
Naval Air Engineering Center
Lakehurst, New Jersey 08733

05 MARCH 1979

Final Report for Period January 1977 through September 1978
AIRTASK A5345342/0514/9534000002

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Prepared for

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AIR-53464
Washington, DC 20361

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APR 2 8 1979

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GOVERNMENT-INDUSTRY DATA EXCHANGE PROGRAM

GENERAL DOCUMENT SUMMARY SHEET

Please Type All Information – See Instructions on Reverse

1. ACCESS NUMBER	2. COMPONENT/PART NAME PER GIDEP SUBJECT THESAURUS
E150-0590	Automated Test Equipment, Circuit Tester, Fault Isolation

3. APPLICATION	4. MFR NOTIFICATION	5. DOCUMENT ISSUE (Month/Year)
Engineering	[ ] NOTIFIED [X] NOT APPLICABLE	Mar 79

6. ORIGINATOR'S DOCUMENT TITLE	7. DOCUMENT TYPE
Integrated Circuit Tester Evaluation Study.	[X] GEN RPT [ ] NONSTD PART [ ] SPEC

8. ORIGINATOR'S DOCUMENT NUMBER	9. ORIGINATOR'S PART NAME/IDENTIFICATION
NAEC-MISC-92-0380	N/A

10. DOCUMENT (SUPERSEDES) (SUPPLEMENTS) ACCESS NO.	11. ENVIRONMENTAL EXPOSURE CODES
None	N/A

12. MANUFACTURER	13. MANUFACTURER PART NUMBER	14. INDUSTRY/GOVERNMENT STANDARD NUMBER
See Box 15	See Box 15	See Box 15

15. OUTLINE, TABLE OF CONTENTS, SUMMARY, OR EQUIVALENT DESCRIPTION

Determines the test requirements and contains the results of a market survey to determine which testers were available that could assist in the detection of faulty integrated circuits. Those that seemed to meet the requirements were to be sent to Naval Air Test Center, Patuxent River, MD for analysis. The testers that performed well in the analysis would then be placed in two AIMD's on a trial basis to determine their usefulness and ease of programming and maintenance under actual working conditions. At the conclusion of these trials, NAVAIRENGCEN would recommend to NAVAIR which tester(s) should be acquired on the basis of cost, utility and operational factors.

Box 12. (MFR)		Box 13. (MFR P/N)	Box 14. (STD NO.)
BENDIX	14892	HERBIE	
BIOMATION	14856	SITEK 2400	
		SITEK 3200	
COMP CONT	----	4050	
		4150	
		4250	
		4350	
		4450	
DATA TEST	50602	4800	
		5800	
FLUKE JOHN	89536	3010A	
		3020A	
		3040A	
GENRAD	24655	1792	
		1795	
		3010A	
HEWLETT-P	04404	5045A	
MACRODATA	51151	MD 154	
		MD 104M	
SANDERS	94117		AN/USM-392
SIEMENS	25088	IT-100	
		IT-200	
		J 721A	

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16. KEY WORDS FOR INDEXING

Integrated Circuit (Doc Des--Q)

17. GIDEP REPRESENTATIVE	18. PARTICIPANT ACTIVITY AND CODE
Frank Sinatra	USN, Naval Air Engineering Center Lakehurst, NJ 08733 (YT)

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3 — Indicate application which the device was used (e.g., ground, missile, shipboard, spacecraft; refer to P & P Manual, Section 13).

4 — Device manufacturer must be notified of test results. Manufacturer approval of report is not required--include pertinent manufacturer correspondence with document submittal to GIDEP; check NOTIFIED entry. If document is for a nonstandard part or of a general nature and a manufacturer is not identified, check NOT APPLICABLE.

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13 — Enter complete part number. Use open O for alpha letter O, and use Ø for numeric zero. If more than one part number, enter phrase, SEE BOX 15; enter additional part number(s). If a part number is not specified, enter four dashes (----).

14 — Enter standard part number such as the 1N or 2N--diode and transistor designators. For GIDEP purposes, any military assigned number is considered as a government standard part number. If more than one standard number, enter phrase SEE BOX 15; enter additional standard number(s).

15 — If subject matter in document can be categorized into more than one major subject category, enter additional subject categories in upper right-hand corner. Briefly summarize test results or material detailed in text of document. Include any pertinent details or comments required for proper interpretation of material presented (e.g., peculiar environmental capabilities, unique electrical characteristics that may be "state-of-the-art," or characteristics that restrict part usage to particular applications or any other details that may aid a prospective user of the part).

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17 — Enter signature or name of GIDEP Representative.

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E150-0590

Box 12. (MFR)		Box 13. (MFR P/N)
SIEMENS	25088	J 724A
		716
		721A
		724A
TERADYNE	23350	J40
		J401
		J133
TESTLINE	51089	2050(AFIT)
WATKINS	14482	ADATE

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I. Summary

A. Purpose:

This report describes the Naval Air Engineering Center's efforts in determining if any commercially available test equipment could assist the Aviation Intermediate Maintenance Department (AIMD) in the detection of faulty integrated circuits (IC's). The test equipment is to isolate IC's both in and out of circuit on avionic printed circuit (PC) boards. Specifically, the Naval Air Engineering Center was to determine the test requirements and conduct a market survey to determine which testers were available to meet these requirements. Those that were deemed to have the potential to accomplish the task specified were to be sent to Naval Air Test Center, Patuxent River, Maryland, for analysis. The testers that performed well in the analysis would then be placed in two AIMD's on trial basis to determine their usefulness and ease of programming and maintenance under actual working conditions. At the conclusion of these trials, NAVAIRENGCEN would recommend to NAVAIR which tester(s) should be acquired on the basis of cost, utility and operational factors.

B. Conclusions:

1. There is a valid testing requirement at the AIMD's that is not satisfied with the current testers.

2. The primary AIMD test requirements for a small, inexpensive, commercially available, digital IC tester could be met by only one tester. This was the automatic Fault Isolation Tester (AFIT) model 2050 manufactured by Testline Co. Many other testers were available that had the basic testing capability but were outside the price constraints or that were edge-board testers. Bed-of-nails testers were not considered for AIMD use. The AFIT was submitted for technical and User Evaluations and demonstrated that it could detect faulty IC's on PC boards not coated with a conformal moisture-proofing compound. This fault detection ability was demonstrated for both the in-circuit and out-of-circuit modes of operation.

3. The conformal moisture-proofing coating applied to avionic Shop Replaceable Assemblies (SRA's) prevents any known tester probe from making consistent, reliable contact with the IC leads. This condition precludes the use of any tester to detect faulty IC's until a probe is available that can pierce the coating. Special probes manufactured by Ostby and Barton Co. (for Testline Co.), for this evaluation, failed.

4. Most Automatic Test Equipment (ATE) presently in the Navy inventory have the basic test capabilities potential necessary for both in-circuit and out-of-circuit digital IC testing. This method could not be used until a probe to penetrate the conformal coating was available. Even with a verified probe this is not considered a viable alternative to a small IC tester.

5. There is no method (technique) for removing the conformal coating, either by chemical or abrasive means, that is suitable for use by the AIMD test personnel (exclusive of the Micro-Min Shop).

6. In order to test any IC on an SRA, it is first necessary to identify its commercial number so that its logical truth table can be determined. Many components mounted on avionics SRA's are marked with contractor's own number. Much effort is required to translate this number to its commercial counterpart.

7. Navy personnel were able to program and operate the Testline AFIT after one week of formal training.

8. The primary function of the AIMD is fleet readiness and other tasks (such as tester evaluations) are performed as work permits. While both Cecil Field and Jacksonville were extremely cooperative, many difficulties arose because of workload scheduling.

C. Recommendations:

1. Do not procure any tester(s) to perform in-circuit testing on conformal-coated PC boards until a successful probe has been demonstrated.

2. NAVAIR to direct NAVAIRENGCEN/NAVAIRTESTCEN to award a competitive contract for the development of a probe to pierce the conformal coating. Verification of the probe (successful completion of the contract) is to be performed by NAVAIRTESTCEN.

3. Do not modify general-purpose ATE to allow testing of components.

4. Conduct limited investigation after a probe is developed to:

a. insure that the test requirements are still valid

b. determine the commercially available testers

5. Do not use an AIMD in future evaluations unless a study of their present and projected workload is analyzed to determine if they can contribute the man-hours to the program without compromising their schedule of tactical repairs.

6. NAVAIR to task NAVAIRENGCEN to evaluate the present system of stocking spares to determine if digital IC's having identical properties are stocked under different numbers. This would alleviate the delay in obtaining the proper component to facilitate the repair.

II. Background

A. Problem:

1. Presently the AIMD utilizes Automatic Test Equipment (ATE) to isolate a failure to a particular Shop Replaceable Assembly (SRA). This ATE

will normally isolate within the SRA to some ambiguity group of discrete components (2 or more). The particular IC responsible for the failure is not normally determined by the ATE due, in part, to Test Program Set (TPS) development cost limitations and test point limitations (initial avionic design restrictions). At this point the procedure to repair the SRA is to:

a. manually probe the board (if technically possible) in order to identify the faulty IC or

b. replace the least reliable IC within the ambiguity group and retest on the ATE, repeat this procedure until successful or

c. replace all IC's in the ambiguity group.

2. The ability and success of the manual probe method is dependent upon the design of the avionics printed circuit (PC) board, the ability of the Navy technician, the availability of probe devices, and the amount of time available for troubleshooting. Because of the variability of the above constraints, this is not a method that can be uniformly applied to all SRA's throughout the AIMD's with a high probability of fault detection.

3. The repair methodology of removing and replacing one IC at a time (normally the least reliable) is the least costly repair method only when the first IC removed is in fact the faulty IC. In all other cases this method consumes critical maintenance assets and manpower, particularly on the ATE. This method is justified only when one component in the ambiguity group has an extremely low reliability in relation to the other components in the ambiguity group.

4. One problem encountered in replacing all the IC's is that spares to replace the entire ambiguity group are sometimes not in stock. Rather than replace a partial amount of IC's, the SRA is taken out of service and waits until the entire group of IC's is available for replacement. Therefore a large amount of spare SRA's are required to be in the pipeline at great expense. In addition, a large amount of spare IC's are required as many good IC's are replaced during this process. Since sparing policy is dependent upon component reliability (expected failure rate), this totally disrupts the supply chain.

5. Another problem complicating the repair cycle is the unknown condition of IC's received from the Navy supply facility. At the present time the maintenance technician must assume the replacement IC is operational because there are no provisions for testing before it is installed on an SRA. The IC can only be tested (on the ATE) as an integral part of the SRA after the repair action is completed. The electronics industry has found that 5% to 10% of incoming IC's were faulty and has been forced (because of cost considerations) to institute an incoming inspection procedure to pass (to the assembly line) only verified IC's. Since the Navy does not verify IC's prior to installing on SRA's, all too often the "fixed" SRA is not operational due to one bad replaced IC. For example, if all IC's have a 5% failure rate and there are 6 IC's in the ambiguity group, there is a 30% probability

of failure when the SRA is retested. At this point the Navy maintenance personnel have followed all instructions and the test still fails. Did the ATE system malfunction, or was one of the replacement IC's faulty? There is no way to determine exactly where the problem is located and large amounts of time, energy, and assets have been committed to a task which ultimately failed.

6. The primary problem is to reduce the diagnostic fault isolation ambiguity group to a single IC. A secondary problem is to verify proper functioning of an IC prior to installation on a PC board. Both of these problems could be resolved by providing the AIMD's the capability to test IC's both in-circuit and out-of-circuit.

B. Scope:

1. NAVAIR recognizes the problem associated with the current test methodologies at the AIMD's and has directed NAVAIRENGCEN (ref (a)) to investigate practical supplementary IC test devices. This investigation is to provide NAVAIR with a support recommendation for fault isolation to the component on avionic PC boards.

2. To accomplish this task, NAVAIRENGCEN initiated an IC Tester Evaluation Program designed to identify a cost-effective solution to the IC problem. This program was divided into four phases:

a. Phase I IC Test Requirements Analysis

b. Phase II - Market Survey and Analysis

c. Phase III - Test and Evaluation

Each Phase was structured to develop all the background information for the following phase. The total evaluation program develops the test requirements and culminates in a recommendation to NAVAIR.

3. The IC tester Evaluation Program was designed to locate and evaluate IC (integrated circuit) testers currently available on the market, to satisfy existing IC test requirements at Navy maintenance sites. The IC Tester Evaluation Program was not intended to become an alternative to normal Test Program Set (TPS) acquisition, but rather an effective way to compensate for unprogrammed test requirements. Such as those occurring as as result of IC ambiguity groups remaining from SRA (Shop Replacement Assemblies) level testing and to insure new IC devices used in repair actions are operable before installation on the SRA.

4. The tasks described above fulfills the requirements of reference (a). In addition, NAVAIRENGCEN initiated independent investigations in the following areas:

a. Incorporation of an IC test probe on existing Navy inventory Automatic Test Equipment, as an alternative to a small new tester.

b. Methods of removing the conformal coating from PC boards at the test station (not in the Micro-Min Shop).

The above investigations were to determine what capability was presently available.

III. Phase I - IC Test Requirements Analysis

A. General:

Test requirements were established by defining the IC test envelope on devices presently in Navy inventory and those planned for introduction in the near future (see Appendix A). Next, test software development problems encountered on ATE systems previously introduced into the fleet were reviewed to determine the minimum hardware/software configuration.

B. Test Requirements:

1. It was determined that a valid testing requirement at the AIMD's exists that cannot be satisfied with the current testers. This requirement is to isolate to the failed component on an SRA.

2. Test Configuration

a. IN-CIRCUIT - The ability to independently test an integrated circuit while installed on an SRA in its normal circuit configuration (without lifting leads, cutting traces, etc.). IN-CIRCUIT test will be on conformal coated PC boards.

b. OUT-OF-CIRCUIT - The ability to test an IC device as received from the supplier prior to its installation on an SRA.

3. Digital IC's

a. IC FAMILIES - 5-volt logic

b. IC CIRCUIT CONFIGURATIONS - Serial and combinational logic

c. TEST METHODS - Parametric and/or functional

d. TEST CAPABILITIES

1. Power Supplies - 5 volts

2. Stimulus - 5 volts

3. Response - 5 volts

4. Interface - 14, 16, 24 pins

4. Physical Description

a. Size - Bench Top

b. Weight - 50 pounds

5. Initial Acquisition/Cost - $20,000/unit

6. Software

a. PROGRAMMING LANGUAGE - Simple and easy to use

b. STORAGE DEVICE - Floppy disk, magnetic tape cassette, PROMs, etc.

IV. Phase II - Market Survey and Analysis

A. General:

1. The purpose of the market survey was first to ascertain what IC testers were commercially available and then to analyze this information to determine what testers met the requirements, as determined in Phase I. Therefore, the survey was initiated by conducting literature searches, attending related conferences and seminars and contacting IC tester manufacturers.

2. This initial segment determined the types of IC testers commercially available and indicated which testers could possibly meet the necessary test requirements. Any testers utilizing a bed-of-nails approach were not considered for this application due to the cost for fixtures. Because of the variety of different PC boards to be tested, the cost of providing these fixtures would exceed by order of magnitude the total target acquisition cost.

3. Each manufacturer meeting the general requirements established in Phase I was asked to send detailed specifications and operating information for evaluation. Upon receipt of this data, each tester was analyzed for technical capability and cost to the Navy. Next, selected vendors were visited to witness a demonstration of testing (both in-circuit and out-of-circuit), review software development techniques, and evaluate operation of self-test software.

These commercially available testers can be classified as to testing characteristics (digital IC testers, small module IC testers, and linear IC testers) and the following discussion has been structured to these classifications (see Appendix B for details).

B. Digital IC Testers:

The market survey indicated that eight testers (from six manufacturers) could possibly meet the test requirements. But analysis of this data determined that only the Testline AFIT model 2050 was capable of providing the test ability required, both in-circuit and out-of-circuit testing. In-

circuit testing is accomplished through a special pulse power test technique patented by Testline. This unit will test most 5-volt logic families and most circuit configurations. Testline has developed a large library of standard IC test programs which are available with the purchase of any AFIT system. Test software to support new IC's can be developed on-site as the need arises, and existing test software may be modified to accommodate special circuit configurations. The dual floppy disk mass storage system provides an on-line test software duplicating capability.

C. Small Module IC Testers:

1. Digital module testers have the necessary stimulus/response repertoire to satisfy both in-circuit and out-of-circuit IC test requirements. But, the test strategy for in-circuit testing must be IC oriented or tailored to satisfy individual IC test requirements. The following general procedure was proposed to satisfy this end:

a. IC power (Vcc) will be applied through normal module input pins.

b. An IC clip connected directly to the IC under test will monitor all IC inputs and outputs.

c. All stimulus signals will be applied to the normal module interface connector and be so constructed as to provide the desired IC input stimulus.

d. The IC in-circuit test program would be limited to the module input stimulus and IC chip response necessary to fully exercise its truth table and evaluate the IC's performance. (IC orientated software).

2. Test software should not be developed for IC's with input-output pins directly accessible through the module interface. (This would be a duplication of SRA test software.)

3. IC test software for digital module testers is more complex for in-circuit testing than is required on standard IC testers since the module tester may have to apply stimulus signals through two or more IC's before it reaches the IC under test.

4. None of the testers evaluated meet the test requirements of Phase I. But the Bendix HERBIE was in the final development stage and, if completed, would meet the requirements. Just prior to the schedule delivery of a HERBIE to NAVAIRTESTCEN (to start Phase III), Bendix advised NAVAIRENGCEN that serious schedule slippages had occurred which would force them to withdraw from the evaluation. Unfortunately this eliminated the only possible small module tester.

D. Linear IC Testers:

Linear IC testers were found to be small, compact, relatively inexpensive devices well suited to maintenance environments. The test

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capability varied from simple operational amplifier/regulator testers with as few as 14 tests to units capable of testing A/D converters with over 28 individual tests. All testers evaluated were limited to out-of-circuit test functions only, in-circuit testing was beyond their capability. As a result linear IC testers were dropped from the evaluation program.

E. Results:

1. This market survey and analysis determined that only one commercially available tester was capable of meeting the testing requirements as defined in Phase I. Arrangements were made to have this tester, Testline AFIT 2050, made available to the, NAVAIRTESTCEN for the Phase III evaluation.

V. Phase III - Test and Evaluation

A. General:

1. The NAVAIRTESTCEN was tasked to test and evaluate the Testline AFIT model 2050. The vendor (Testline) supplied a tester and provided the evaluating personnel with operating test software development and maintenance training (at no cost to the government). This Test and Evaluation program consisted of:

a. Verifying the tester's ability to perform in-circuit and out-of-circuit test functions.

b. Evaluating the capability of developing new IC test software.

c. Evaluating the capability to modify existing test software.

d. Verifying ease of performing scheduled and unscheduled maintenance.

2. The NAVAIRTESTCEN has conducted a preliminary evaluation of the AFIT during the time frame of 19 Jan to 12 Apr 1976 (ref (b)). In addition, a method for dry blasting the PC boards to remove the conformal coating, was evaluated. This dry blast method was found "not suitable for providing a means of removing the moisture preventive coating from Navy Shop Replaceable Assemblies ..." (ref (c) page 5).

B. T&E Conclusions

1. The conclusion of the T&E effort (ref (c) page 5), was that: "The Automatic Fault Isolation Tester can adequately detect faulty Integrated Circuits when used as both an in-circuit/out-of-circuit Integrated Circuit Tester; however; the correction of the three Phase II deficiencies will greatly enhance its operation and maintenance."

2. The three deficiencies cited above were:

a. "Interference of the Automatic Fault Isolation Tester test clip with Navy Shop Replaceable Assembly bus bars."

b. "Failure of the test clip to penetrate the moisture protective coating."

c. "Ability to test only 5V logic."

C. T& E Recommendations (ref (c)):

"Procure the Automatic Fault Isolation Tester for intermediate level maintenance support for Navy Shop Replaceable Assemblies containing Integrated Circuits."

D. NAVAIRENGCEN Action:

1. In an effort to solve two of these problems, NAVAIRENGCEN discussed with Testline the possibility of designing a new probe which would reliably pierce the moisture proofing on the SRA and not be prevented from making contact because of components or bus bars mounted in close proximity to the IC under test. Testline, in cooperation with the Ostby and Barton Co., developed a new probe specifically designed to penetrate the moisture proofing compound on Navy PC boards. The probe consisted of:

a. needle point pins that are spring loaded for 8 oz. (14- and 16- pin configurations, expandable to 32 pins).

b. A pin mounting device with a guide block (to protect the pins) and an edge guide (for proper alignment on the chip); pins are set at 10° from the vertical.

c. A drill-press type arrangement to bring the pins into continuous contact with the leads (without the requirement of holding the chip).

2. The Testline Co. integrated this probe device on an AFIT. NAVAIRENGCEN made arrangements to have the AFIT evaluated at two working AIMD's under actual shop conditions(Phase IV).

VI. Phase IV - User Evaluation

A. General:

1. Only one tester from Phase II, the Testline AFIT model 2050, met the test requirements of Phase I and was found satisfactory for Intermediate Level Maintenance by NAVAIRTESTCEN (Phase III). The final evaluation (Phase IV) was designed to determine the technical abilities of the AFIT under normal AIMD shop conditions. During this evaluation all operation and software development would be performed by Navy personnel assigned to the AIMD. All testing would be performed on avionic SRA's (conformal coated). This is the environment for which the tester is being considered.

2. It was decided to execute concurrent evaluations at two AIMD's under different test conditions and combine the results to form a composite analysis. The AIMD's selected were:

a. NAS Cecil Field, FL - to test S-3 PC boards after an ambiguity group had been identified by the HATS testers, components will be mostly Dual-in-line-plastic (DIP) with some flat-packs.

b. NAS Jacksonville, FL - to test P-3 PC boards not previously tested by ATE (ambiguity group is the entire board), components will be mostly flat-packs with some DIP's.

A composite analysis of the tester's capabilities on avionic SRA's at these AIMD's will constitute a good representation of the true Navy working environment.

B. Method of Evaluation:

1. The evaluation plan was constructed to enable analysis of:

a. Programming - ease in modifying existing programs and difficulty associated with constructing new programs.

b. SRA's tested on IC tester by type and quantity of IC's tested, to evaluate the ability to isolate to the failed component and the time necessary to accomplish this.

c. SRA's from HATS not tested on IC tester - used to establish a basis of comparison for time, cost, and resources consumed.

d. Tester Reliability and Maintainability - to determine Mean Time Between Failure (MTBF) and to pinpoint maintainability problems.

e. Component Spares - out-of-circuit testing of the spare stock of IC's to determine percentage of defectives received from the vendor, attempt to extrapolate this percentage to a cost to the Navy.

2. Appendix C is the NAVAIRENGCEN's AFIT evaluation plan and explains the information to be collected (logs), that are needed to provide the analysis information listed above.

C. AIMD Cecil Field Evaluation:

1. Two Navy personnel from the AIMD attended one week of programming and operating training at the Testline factory at Titusville, Florida (all training during this evaluation was furnished by Testline at no cost to the government). The following week (on 25 April 1978) an AFIT was installed. During the initial familiarization stage, the Navy technicians broke 5 pins on the newly designed probe. This downed the probe while awaiting spare pins. It was determined that the pins broke becuase of a sideward force on the pin tip. This force was generated by the pins slipping off the leads due to:

a. IC chips (and leads) not being all exactly the same size.

b. Pins (on the probe) not being exactly the same distance from the center line (poor quality control).

2. Testline, upon being informed of failure of the probe to operate reliably, proceeded to redesign it to improve its effectiveness. On 2 August 1978 a newly designed, hand-held version was delivered to Cecil Field. Unfortunately this probe utilized the same type pins that were used in the original design. These pins were used on approximately 20 IC's before they started to fail. After testing two SRA's, most of the 16 pins were deformed and bent. An effort was made to replace these pins and spare ones, but no positive results could be achieved with the probe.

3. During the interim, before receiving the second new probe, the technicians used the AFIT with SRA's which had not received a moistureproof coating (non-tactical printed circuit boards) and utilized the standard probe. Only a limited amount of testing was actually performed. Based upon this small sample, it was found that:

a. sailors have the ability to program the AFIT.

b. The AFIT detects and fault isolates in-circuit defective IC's.

D. AIMD Jacksonville Evaluation:

1. The AFIT was installed at the AIMD at JAX on 20 June 1977. As was the case with Cecil Field, two Navy technicians attended the Testline class one week prior to installation. Although Testline was given a sample of the P-3 boards being tested and had stated that they had a flat-pack type probe to pierce conformal coating, none was delivered with the tester. Upon inquiry, no assurance was given that one would be available in the near future. As an interim solution, a standard flat-pack probe was obtained from Testline and used at both Jacksonville and Cecil Field. At Cecil Field this probe was not able to make contact with all 14 or 16 pins simultaneously in test after test. At Jacksonville some limited success was achieved, but it was felt that consistent results at various sites could not be obtained with this probe.

E. Results:

1. The user evaluation was cancelled at both AIMD's during the week of 4 September 1978. This cancellation was due to the fact that probes were not available that would consistently and successfully penetrate the conformal coating and, therefore, an evaluation of the tester under operating conditions could not be obtained. In addition, all probes failed so quickly that the data to fill in the logs was not obtained. No real evaluation of the tester itself could be made but it appears that the AFIT will isolate to the faulty component.

2. The NAVAIRENGCEN contacted probe manufacturers to determine if they had a product that could pierce the moisture proofing or could develop such a probe. No company would offer to undertake an assignment of this type because they felt that, due to past experience, no such device was possible. The Pylon Corp. had developed a probe that had heated pins (600° F)

which vaporized the coating, exposing the leads. The problem was in using only enough heat, otherwise the hot pins melted the solder and could also go through the leads. The Pylon Corp. considers this probe as a laboratory tool, not a general-purpose device.

3. When (if) a probe is developed, it will have to be deployed in various configurations to mate with the variations in IC configurations. There are at least three different configurations of Dual-In-line IC's (Hermatic, Ceramic, and Plastic) which could require different probes. Flat packs come in at least two different configurations. In addition, within configurations, manufacturers vary the length of the leads on the IC.

4. A number of problems arose at both AIMD's during the evaluation because of the attempt to successfully perform the AIMD mission while conducting an evaluation. Both AIMD's were apparently under-staffed and were experiencing extremely heavy work loads during the evaluation period. All officers and enlisted personnel at Cecil Field and Jacksonville were very cooperative but their primary responsibility is to fleet readiness. Additional tasks are performed as work permits. Of the original four Navy technicians trained for the AFIT, one was transferred out of the AIMD during the evaluation. The other three were assigned to various shifts to coincide with their primary AIMD assignments. While utilization of actual AIMD's does get down to the reality of true operating conditions, this was not felt to be the best environment for a tester evaluation. Future evaluations should be under more controlled conditions so that the tester receives the resources necessary.

5. In order to test the particular IC, it is first necessary to identify its commercial number so that its logical truth table can be determined. Navy components counted on avionics SRA's are marked with the contractor's own number. NAVAIRENGCEN went back to the contractor and obtained the translation of this number to its commercial counterpart. This procedure was used for this evaluation only and would not be practical for large-scale implementation. Two alternatives are practical:

a. Mark all components with the standard commercial number, this could be in addition to the contractor's number.

b. Have available at all AIMD's (as part of the TPS) a translation document that will supply the commercial equivalent of the contractor's number.

6. A more comprehensive solution to the above problem entails a study of Federal Stock Numbers (FSN) assignment. Under the present system, all manufacturers of avionics can assign a proprietary company number to a standard IC if they desire any different parameter from the stock IC. This proprietary number, usually called a Specification Control Drawing (SCD), is assigned because some extra testing of the IC is requested, or because one or more of the parameters are to be held to narrower limits than usual, or for some other variation from the standard configuration, it has a unique FSN. A study could determine which SCD's can be interchanged due to the fact that the individual differences are not beyond the specifications of their circuit

requirements. It might be demonstrated that many FSN's (for IC's) are redundant and the quantity of different spare IC's required could be reduced. This would result in a large cost savings and could improve turn-around-time in the repair of SRA's.

7. The Testline AFIT did demonstrate the ability to fault isolate to the failed component for non-conformal coated SRA's. Therefore, this tester could be used in the Micro-Min Shop after the coating was removed. This possibility is outside the realm of this investigation as it is not a question of can it perform the task, but rather, where should it be performed. Implementation of this mode of operation would require a restructing of the areas of responsibility within the AIMD.

VII. Independent Investigations

A. Utilize Existing ATE

1. The ATE, in the AIMD, will normally isolate to some ambiguity group of 2 or more discrete components. The particular defective IC is not normally isolated by the ATE because of TPS cost limitations, avionics design restrictions and the physical inability to isolate from the edge-board connections. Most ATE have the basic test capabilities potential necessary for both in-circuit and out-of-circuit digital IC testing. The incorporation of a probe onto existing ATE is a possible alternative to procuring a small new tester. Informal discussions were held with the following companies to discuss this possibility:

a. General Dynamics - HATS

b. AAI - 5556

c. Sperry - DIMOTE II A

d. Grumman-CAT III D

2. A general evaluation of the technical feasibility of supporting IC maintenance test requirements on inventory ATE was conducted. This evaluation covered ATE systems:

a. Stimulus/Response Repertoire: This stimulus/response capability of each ATE system was reviewed to determine the level of compatibility between existing ATE systems and IC test requirements. Each system was found to contain more test capability than is needed and, therefore, could satisfy current maintenance test requirements.

b. Test Software Development: The test software development methodology used on each system was WRA/SRA oriented. In order to utilize these systems in a cost-effective, efficient manner, the IC test software development methodology must be adopted and integrated into the assembly oriented methodology for all in-circuit test requirements.

c. Modification of SRA Test Software: The modification of existing SRA test software to include in-circuit IC testing was found to be impractical and very costly. SRA test software has been developed to support assembly level testing, applying stimulus through the SRA connector and monitoring responses through the same connector with little or no probing. For any set of stimulus inputs, the SRA outputs are known but the individual IC in-puts and out-puts are not easily determined without an in-depth analysis. Also, depending on the SRA complexity, the stimulus required to exercise one IC may be buried in stimulus for a number of other IC's thus limiting the usability of existing software. IC test stratogems are based on the IC's truth table. In general, IC test sequences, even for those IC's buried in complex circuits, are much simpler and easier to develop than those used for SRA level testing.

d. Interconnecting Device (ID) Requirements: Each system studied will require an ID for out-of-circuit testing which can be satisfied by using a universal probe capable of handling 14-, 16-, 24-, 32- pin configurations. In-circuit requirements (IC clips) may be incorporated into existing ID's or adapters or may be designed into a new assembly (existing ID/adapter hardware should not be duplicated).

e. Station Availability: The detailed data required to make an effective assessment of station time available for IC testing on each ATE system was not readily obtainable due to:

(1) Great variations between AIMD's,

(2) Cyclic nature of the work load, and

(3) General lack of current and projected data.

3. All ATE studied could be modified to accept a probe and could successfully test digital IC's. All the electronics, computer, and storage devices are in place to perform the testing. All manufacturers stated that the Government must furnish a probe as they did not know of one capable of penetrating the conformal coating. Since such a probe does not exist, this is not currently a possibility.

4. The basic question is not whether ATE is capable of testing components, but rather should a general-purpose automatic test station be utilized to test components. Current Navy inventory testers could be easily modified to accept an IC probe and isolate to the failed component, however, no specific piece of ATE (exclusive of VAST which was not considered) exists at more than 25% of the AIMD's. Even if this testing requirement is limited to sites with general-purpose ATE, the same ATE is not at all those sites. Therefore, either:

a. More of one particular ATE must be procured, or

b. Similar software must be developed for more than one piece of ATE.

However, "a" is a totally impractical solution due to acquisition cost, and "b" is not cost effective and would lead to a software configuration management problem. Therefore, utilizing ATE to test components is not a viable alternative to a small IC tester.

5. While definite station time availability is not known, direct observation of SIMD operations indicate that time is not normally available. The current NAVAIR policy is to place new avionics on existing ATE whenever feasible. Therefore, even if time were available today it probably will not be available in the future.

B. Conformal Coating

1. A market search was conducted to see what methods were available to remove the conformal coating from individual components, from larger areas or from the entire PC board. This search was concerned only with those methods (techniques) that could be used at the test bench, not in the Micro-Min Shop.

2. The only method that appeared feasible was the Zero dry blast cabinet manufactured by the Zero Manufacturing Co. This blaster is designed for dry blasting small or intricate parts to produce a metallurgically clean surface. The blaster can utilize all types of fine abrasives. To evaluate its capabilities a blaster was obtained (no cost to the government) and shipped to the NAVAIRTESTCEN for evaluation with the AFIT (as Phase III).

3. The evaluation of this blaster (reference (c)) determined that it had 2 major deficiencies:

a. "when dry blasting an SRA, the abrasive, glass beads, used to remove the moisture protective coating, also removed printed circuit runs, pads, and component identifications."

b. "the filter screen basket permits large particles of debris to pass through and enter into the storage hopper. This caused the blasting gun to clog frequently."

4. The Zero dry blast cabinet is not suitable for removing the conformal coating from SRA's.

5. There is no method for removing the conformal coating, either chemical or abrasive means, that is suitable for use by the AIMD test personnel (exclusive of the Micro-Min Shop).

VIII: References

(a) NAVAIR ltr 53424/MDM Ser 114 of 19 Jan 1977: ATE IMRL Change; Request for
(b) NATC Report of Test Results SY-165R-76 of 26 Jul 1976: Test and Evaluation of the Automatic Fault Isolation Tester (AFIT), First and Final Report
(c) NATC Report of Test Results SY-36R-78 of 31 Mar 1978: Test and Evaluation of the Automatic Fault Isolation Tester in conjunction with the Zero Dry Blast Cabinet; 1st Report (Final)

APPENDIX A

ESTABLISHMENT OF TEST REQUIREMENTS

APPENDIX A

ESTABLISHMENT OF TEST REQUIREMENTS

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APPENDIX A

Establishment of Test Requirements

I. IC Test Requirements

IC test requirements were initially established to support existing hardware, presently in Navy inventory, plus those requirements anticipated for future hardware. As IC tester characteristics data was compiled it became clear no one tester on the market could satisfy all of these requirements. This resulted in a reassessment of the basic test requirements to find the minimum acceptable test requirements envelope for maintenance support testing.

II. Initial Requirements

Test requirements were established by defining the IC test envelope on devices presently in Navy inventory and those planned for introduction in the near future. Next, test software development problems encountered on ATE systems previously introduced into the fleet were reviewed to determine the optimum hardware/software configuration. The results of these two efforts are summarized below:

Test Configurations

- IN-CIRCUIT - The ability to independently test an integrated circuit while installed on an SRA in its normal circuit configuration (without lifting leads, cutting traces, etc.).
- OUT-OF-CIRCUIT - The ability to test an IC device as received from the supplier prior to its installation on an SRA (also referred to as a device testing).

Digital ICs

- IC FAMILIES - TTL, DTL, RTL, ECL, CMOS, PMOS, NMOS, memory chips etc.
- DIGITAL CIRCUIT CONFIGURATIONS - Shift registers, counter gates, flip-flops, priority encoders, Schmitt triggers, parity generators/checkers, decoders/encoders, arithmetic logic units, etc.; in SSI, MSI, and LSI configurations.
- TEST METHODS - Parametric and functional
- TEST CAPABILITIES - Power Supplies - 0 to ±20 volts (programmable in 100 millivolt steps).
  Stimulus - 0 to ± 18.75 volts (programmable)
  Response - 0 to ± 18.75 volts (programmable)
  Interface - 32 pins (expandable to 64 pins)

. PHYSICAL DESCRIPTION

Size - Bench Top
Weight - 50 pounds (maximum)

Linear ICs

. CIRCUIT CONFIGURATIONS - Operational amplifiers, differential amplifiers, sense amplifiers, comparitors, voltage followers, voltage regulators, etc.

. TEST CAPABILITY - Power Supplier - 0 to ± 50 volts (programmable)
Stimulus - 0 to 50V @ 0 to 20V/μs slew rate
Measurement - 0 to 200V @ ±1%, 0 to 200MA @ ±1%
Loads - 50 to 100K
Interface - 32 pins
Type Testing - DC and AC parametric

. PHYSICAL DESCRIPTION

Size - Bench Top
Weight - 50 pounds (maximum)

Cost

Initial hardware acquisition cost shall not exceed $20,000 per unit.

Software

. On-line test software development

. Simple, easy to use language

. Test software stored on floppy disk, magnetic tape cassette, or PROMs.

III. Final Test Requirements

The initial IC test requirements specified above were found to be impractical after the initial hardware survey was completed. The study revealed most testers were designed to support limited test requirements for various production and incoming inspection functions, rather than the broad test functions required to support maintenance sites. As a result tester requirements were revised as summarized below:

Test Configuration

. IN-CIRCUIT - The ability to independently test an integrated circuit while installed on an SRA in its normal circuit configuration (without lifting leads, cutting traces, etc.).

. OUT-OF-CIRCUIT - The ability to test an IC device as received from the supplier prior to its installation on an SRA.

Digital ICs

. IC FAMILIES - 5 volt logic

. IC CIRCUIT CONFIGURATIONS - Serial and combinational logic

. TEST METHODS - Parametric and/or functional

. TEST CAPABILITIES

Power Supplies - 5 volts
Stimulus - 5 volts
Response - 5 volts
Interface - 14, 16, 24 pins

. PHYSICAL DESCRIPTION

Size - Bench Top
Weight - 50 pounds

Cost

. INITIAL ACQUISITION - $20,000/unit

Software

. PROGRAMMING LANGUAGE - Simple and easy to use

. STORAGE DEVICE - Floppy disk, magnetic tape cassette, PROMs, etc.

APPENDIX B

MARKET SURVEY DATA AND ANALYSIS

Testers covered in this appendix represent the final group selected for analysis. A detailed data sheet for each selected tester is presented herein. Other testers originally considered and eliminated during the initial vendor evaluation are not included as this would only add to the bulk of the report and serve no useful purpose.

APPENDIX B

MARKET SURVEY DATA AND ANALYSIS

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APPENDIX B

MARKET SURVEY DATA AND ANALYSIS

I. General

A. A market survey was conducted to determine the capabilities of IC testers currently available in industry and to determine their ability to meet the testing requirements of the AIMD's. During the initial phase of this program, maintenance test requirements were optimized to provide maximum coverage of all IC families currently in Navy inventory. Although this was a theoretically sound approach, it proved to be impractical. Each IC tester currently on the market was found to have been designed for a specific test need (production in-process testing, production completed assembly (Q.A.) testing, user incoming inspection testing, and maintenance testing), and therefore, did not meet the overall general requirement to establish a Navy maintenance tester. As a result the test requirements were reviewed to determine the minimum acceptable test characteristics required to support the majority of IC maintenance actions currently encountered. Each tester was then re-analyzed against this new set of test characteristics but only one tester was found to satisfy the minimum test requirements and it showed some evidence of having minor implementation problems which would require minor hardware modifications.

B. In an effort to find a more viable solution the evaluation program was expanded to include small automatic digital module testers. Each tester considered was evaluated against the minimum test requirements established for IC testers. The results of this effort was similar to those experienced for IC testers. The initial acquisition cost and/or relative life cycle costs exceeded the ceiling price. Only one digital module tester was found to meet the minimum test/cost requirements. But, as with IC testers, showed evidence of having minor implementation problems which would require minor hardware modifications.

II. Market Survey

A. Introduction

The market survey and analysis covered digital IC testers, linear IC testers and small digital module IC testers in its search for a cost effective solution to IC test requirements in a maintenance environment. Annex A contains a description, test characteristics, and analysis of each tester evaluated during Phase II of this study.

B. Digital IC testers

The market survey began by contacting over twenty manufacturers of IC testers to determine the basic operating characteristics of testers

currently available on the market. Those which appeared to meet the general IC test requirements were asked to supply detailed operating characteristics and application notes on each tester. (Most responses to this request came in the form of standard sales brochures.) Analysis of this data indicated IC testers broke down into the following test application catagories:

- In-process production
- Completed assembly (device)
- Incoming inspection
- Maintenance/repair

IC testers appear to have been designed to satisfy the specific and unique test requirements of each catagory.

1. In-Process Production Testers

In-process testers are designed to perform various production test functions at the chip or wafer level prior to final assembly and encapsulation. Test access is normally accomplished through probe interfaces and in most cases have multiple head assemblies. They are normally large expensive assemblies which require off-line test software development. The in-process production IC testers were dropped during the initial evaluation phase because they did not have an in-circuit test capability, were large and bulky, and they exceeded the initial acquisition ceiling set by NAEC.

2. Completed Assembly Production Testers

Completed assembly or production QA testers were found to be designed to test large quantities of ICs at a high rate of speed. But each tester was found to support a limited variety of IC devices. The testers are normally loaded by manually inserting into multiple heads or may be used in conjunction with a number of automatic handlers. The latter automatically segregates good and bad ICs and can, through special tester programming, segregate ICs according to their failure mode. Most testers in this group collect production data and display failure data. As a general rule, most testers evaluated required 1 or 2 hardware programming boards to set test parameters and perform the necessary interface wiring. (The average IC/program board ratio was found to be approximately 2 to 1.) When a limited variety of ICs are to be tested this appears to be a reasonable approach, but when a large variety of ICs are considered, the number of programming boards become a significant life cycle cost element. Programming boards contain an element which makes them undesirable for maintenance applications; it is known as a reference device or "known good" device. All testing assumes this device is operational and none of the testers evaluated contain provisions to verify the condition of the "known good" device prior to initiation of production testing.

Two of the testers evaluated were software based machines as opposed to the hardware based machines previously described. But, neither of these contained an on-line test software development capability. All test software was

developed at the suppliers software development facility. This increased life cycle cost and eliminated the autonomous operation desired at maintenance sites.

None of the testers evaluated in this group (figure B1) were found to have an in-circuit test capability. All testers in this group were eliminated from further consideration due to their high acquisition cost and/or high life cycle cost and their inability to test ICs in an in-circuit test configuration.

3. Incoming Inspection Testers

Incoming inspection IC testers (figure B2) offered a wide variety of approaches to IC testing from manual units to fully automated units providing parametric test functions in addition to an assortment of functional test techniques. Two of the testers use manual controls to set up test parameters and simple program boards to provide UUT and "known good" device interface wiring. Test instructions and control settings are contained in test procedures or test documents. The remaining hardware based testers use program boards to set test parameters, house "known good" device, and perform interface wiring functions. The testers do not contain provisions for testing or verifying the "known good" device prior to initiation of the normal test sequence. Software based testers require off-line test software development which significantly increases the life cycle of these units as did the program board requirement for hardware based testers. Two of the testers evaluated in this group are designed to test linear circuits as well as digital ICs. As seen with other groups evaluated, incoming inspection testers are limited to out-of-circuit test configurations only. This limitation plus the high acquisition and/or life cycle cost resulted in this entire group being dropped from further consideration.

4. Maintenance Testers

The last group of IC testers (figure B3) were designed specifically to support maintenance test requirements. This group contained only one tester, Testline's AFIT (model 2050). AFIT was the only IC tester evaluated capable of providing in-circuit and out-of-circuit test functions. In-circuit tests are accomplished through a special test technique patented by Testline. This unit will test most 5 volt logic families and most circuit configurations. Testline has developed a large library of standard IC test programs which are available with the purchase of any AFIT system. Test software to support new ICs can be developed on-site as the need arises and existing test software may be modified to accommodate special circuit configurations. The dual floppy disk mass storage system provides an on-line test software duplicating capability. This tester met the minimum test requirements set forth in Appendix A. The analysis did uncover two utilization problems:

1. The IC clips used during in-circuit testing can not penetrate the conformal coating normally used on avionics SRAs.

2. The tester cannot verify IC clip contact prior to initiation of the normal test sequence.

In spite of these limitations AFIT was the only IC tester found to meet the minimum maintenance test requirements.

C. Digital Module Testers

1. General

a. The requirement for in-circuit testing reduced IC tester candidates to one tester having a limited test range (5 volt logic only). In an effort to find a more viable solution the evaluation was expanded to small digital module testers. This was a natural expansion since module testers have the basic technology to test ICs in both in-circuit and out-of-circuit configurations.

b. Digital module testers have the necessary stimulus/response repertoire to satisfy both in-circuit and out-of-circuit IC test requirements. But, the test strategy for in-circuit testing must be IC oriented or tailored to satisfy individual IC test requirements. The following general procedure was proposed to satisfy this end:

(1) IC power (Vcc) will be applied through normal module input pins.

(2) An IC clip connected directly to the IC under test will monitor all IC inputs and outputs.

(3) All stimulus signals will be applied to the normal module interface connector and be so constructed as to provide the desired IC input stimulus.

(4) The IC in-circuit test program would be limited to the module input stimulus and IC chip response necessary to fully exercise its truth table and evaluate the ICs performance. (IC oriented software)

(5) Test software should not be developed for ICs with input/output pins directly accessible through the module interface. (This would be a duplication of SRA test software.)

c. IC test software for digital module testers is more complex for in-circuit testing than is required on standard IC testers since the module tester may have to apply stimulus signals through two or more ICs before it reaches the IC under test.

d. As with IC testers, module testers were found to be designed to satisfy specific test requirements. But the boundries between production, incoming inspection and maintenance are less decernable and there is more overlap from one group of testers to another.

2. Production Module Testers

Production module testers (figure B4) are designed to provide performance verification and diagnostic fault isolation tests. Diagnostic software for this application is expanded to include test routines designed to identify unique problems encountered during module assembly (solder splashes, shorted traces, spin traces, open lands, open feed-thrus, etc.). Inclusion of these routines increases manual probing operations and the number of operator instructions beyond the level normally considered acceptable in a maintenance operation. Software repair instructions to the operator contain large ambiguity groups which, in most cases, must be resolved manually off-line. The testers evaluated in this catagory presented a wide variety of test methodologies from transition counters to pattern comparitors using "known good" device comparitors and pattern library comparison techniques. Test software storage mediums varied from magnetic cards (the size of standard credit cards) to large moving head disk systems. In general, the production module tester was much larger and contained more test capability than those used in maintenance applications. Testers in this group are technically capable of satisfying IC in-circuit and out-of-circuit test requirements, but are generally much larger than a bench top tester and there initial acquisition cost and/or life cycle cost exceeded the ceiling price of this program.

3. Maintenance Module Tester

a. Module testers (figure B5) designed to support maintenance test requirements were found to be smaller and less sophisticated than production testers. Their test capability varied from TTL logic testers to units capable of testing all logic families in both parametric and functional modes. Test software storage mediums also appear in a variety of technologies from paper tape to PROM assemblies, with floppy disk being the one most commonly used. The initial acquisition cost of these units in most cases was much greater than the unit ceiling price. Testers which come close to or met the unit cost ceiling price exhibited evidence of having relatively high life cycle costs, except one tester, Bendix model 13A9070 (HERBIE). The acquisition cost of this tester is under $12,000. In addition, HERBIE'S life cycle cost elements appear to be reasonable since all test programs are developed on-site by Navy maintenance personnel and interface required (IDs) are relatively simple.

b. The Bendix model 13A9070 module tester is limited to 5 volt logic, but this covers most logic families currently used in avionic

systems. Its programming language and machine language are simple and easy to use with minimum training. Self test on this unit provides diagnostic fault isolation down to the component level of repair. The Bendix model 13A9070 was selected for Phase III testing because it satisfied the test requirements specified in Appendix A, was well under the program price ceiling, and had a relatively low life cycle cost.

c. All module testers, even those designed specifically for maintenance applications, have trouble testing SRAs covered with standard conformal coating. The IC clips commonly used cannot penetrate this coating. Bendix agreed to solve this problem by modifying their tester to provide:

(1) An IC clip assembly capable of penetrating the SRA conformal coating.

(2) A method of verifying IC clip contact prior to initiation of test sequence.

These features were scheduled to be implemented and verified prior to HERBIES shipment to NATC.

d. During Phase II of this evaluation, Bendix was in the final development phase of HERBIE. Production had started on some assemblies and the remaining assemblies were scheduled to start production within a time frame which was compatible with Phase III of the evaluation program. Just prior to the scheduled delivery of HERBIE to NATC, Bendix advised the evaluation coordinator of serious schedule slippages which would force them to withdraw from the evaluation. Unfortunately, this left the evaluation program with only one tester for Phases III and IV.

D. Linear IC Testers

Linear IC testers were found to be small, compact, relatively inexpensive devices well suited to maintenance environments. The test capability varied from simple operational amplifier/regulator testers with as few as 14 tests to units capable of testing A/D converter with over 28 individual tests. All testers evaluated were limited to out-of-circuit test functions only, in-circuit testing was beyond their capability. As a result linear IC testers were dropped from the evaluation program.

DIGITAL IC DEVICE TESTERS

(PRODUCTION - Final Test)

	BIOMATION SITEK 3200	MACRODATA MD 104M	MACRODATA MD 154	TERADYNE J40
INTERFACE	14 - 34 pin	14 - 32 pin	48 pin	14 - 24 pin
PROG. BOARDS	YES	N/A	N/A	N/A
REF. DEVICE	YES	NO	N/A	NO
SOFTWARE	N/A	OFF-LINE	ON-LINE	ON-LINE
IC TYPES	ALL	ALL	LSI	TTL
INPUT PWR.	115V @ 2A	115V	-----	115V
STIMULUS	PSEUDO-RANDOM	STORED PATTERN	STORED PATTERN	STORED PATTERN
RESPONSE	R/D COMPARE	STORED PATTERN	STORED PATTERN	STORED PATTERN
TEST DEVEL. DOC.	SPEC SHEET	SPEC SHEET	SPEC SHEET	SPEC SHEET
TYPE TEST	FUNC/PARA	FUNC/PARA	FUNC/PARA	FUNC/PARA
SELF TEST	YES*	YES	YES	YES
PHYS. DESC.	BENCH TOP	BENCH TOP	2 BAY	BENCH TOP
IN-CIRCUIT TEST	NO	NO	NO	NO

*DOES NOT INCLUDE PROGRAMMING BOARDS

Sheet 1 of 2

FIGURE B1

DIGITAL IC DEVICE TESTERS

(PRODUCTION - Final Test)

	721A	SIEMENS 724A	IT-100
INTERFACE	14 - 16 pin	14 - 24 pin	14 - 48 pin
PROG. BOARDS	YES	YES	N/A
REF. DEVICE	YES	YES	NO
SOFTWARE	N/A		FACTORY
IC TYPES	ALL	ALL	ALL
INPUT POWER	115V	115V	115V
STIMULUS	GREY CODE	GREY CODE	STORED PATTERN
RESPONSE	R/D COMPARE	R/D COMPARE	STORED PATTERN
TEST DEVEL. DOC.	SPEC SHEET	SPEC SHEET	SPEC SHEET
TYPE TEST	FUNC/PARA	FUNC/PARA	FUNC/PARA
SELF TEST	YES*	YES*	YES
PHYS. DESC.	BENCH TOP	BENCH TOP	BENCH TOP
IN-CIRCUIT TEST	NO	NO	NO

*DOES NOT INCLUDE PROGRAMMING BOARDS

Sheet 2 of 2

FIGURE B1

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DIGITAL IC DEVICE TESTER
(INCOMING INSPECTION)

	BIOMATION		TERADYNE		HEWLETT PACKARD
	SITEK 2400	SITEK 3200	MODEL J401	MODEL J133	HP 5045A
INTERFACE	14 - 24 pin	14 - 24 pin	14 - 24 pin	14 - 24 pin	14 - 34 pin
PROG. BOARDS	2	2	N/A	2	N/A
SOFTWARE			ON-LINE		FACTORY
REF. DEVICE	YES	YES	N/A	YES	N/A
IC TYPES	5V LOGIC	ALL	TTL		ALL
INPUT POWER	115V @ 1.5A	115V @ 2A	115V	115V	115V
STIMULUS	PSEUDO RANDOM	PSEUDO RANDOM	STORED PATTERN	GREY CODE	STORED PATTERN
RESPONSE	R/D COMPARE	R/D COMPARE	STORED PATTERN	R/D COMPARE	STORED PATTERN
TEST DEVEL. DOC.	SPEC SHEET	SPEC SHEET	SPEC SHEET	SPEC SHEET	SPEC SHEET
TYPE TEST	FUNC	FUNC/PARA	FUNC/PARA	FUNC/PARA	FUNC/PARA
SELF TEST	YES*	YES*	YES	YES*	YES
PHYS. DESC.	BENCH TOP	BENCH TOP	5 UNIT CONS.	BENCH TOP	BENCH TOP
IN-CIRCUIT TEST	NO	NO	NO	NO	NO

*DOES NOT INCLUDE PROGRAMMING BOARDS

FIGURE B2

DIGITAL IC DEVICE TEST
(INCOMING INSPECTION)

	SIEMENS			
	716	721A	724A	IT-200
INTERFACE	14 - 24 pin	14 - 16 pin	14 -24 pin	14 - 48 pin
PROG. BOARDS	2	2	2	N/A
SOFTWARE				FACTORY
REF. DEVICE	YES	YES	YES	N/A
IC TYPES	ALL	ALL	ALL	ALL
INPUT POWER	115V	115V	115V	115V
STIMULUS	GREY CODE	GREY CODE	GREY CODE	STORED PATTERN
RESPONSE	R/D COMPARE	R/D COMPARE	R/D COMPARE	STORED PATTERN
TEST DEVEL. DOC.	SPEC SHEET	SPEC SHEET	SPEC SHEET	SPEC SHEET
TYPE TEST	FUNC/PARA	FUNC/PARA	FUNC/PARA	FUNC/PARA
SELF TEST	YES*	YES*	YES*	YES
PHYS. DESC.	BENCH TOP	BENCH TOP	BENCH TOP	BENCH TOP
IN-CIRCUIT TEST	NO	NO	NO	NO

*DOES NOT INCLUDE PROGRAMMING BOARDS

FIGURE B2 (CONT)

DIGITAL IC DEVICE TESTER

(MAINTENANCE)

	TESTLINE 2050 (AFIT)
INTERFACE	14 - 32 pin
PROG. BOARDS	N/A
SOFTWARE	ON-LINE
REF. DEVICE	N/A
IC TYPES	5V LOGIC
INPUT POWER	115V
STIMULUS	STORED PATTERN
RESPONSE	STORED PATTERN
TEST DEVEL. DOC	SPEC SHEET
TYPE TEST	FUNC
SELF TEST	YES
PHYS. DESC.	BENCH TOP
IN-CIRCUIT TEST	YES
DEVICE TEST	YES

FIGURE B3

DIGITAL MODULE TESTERS
(PRODUCTION)

	GEN RAD 1792	1795	FLUK TRENDAR 3010A	3020A	3040A
CONNECTOR	60 pins	72-480 pins	128 pins	128 pins	256 pins
INTERFACE	BI-DIRECT	BI-DIRECT	BI-DIRECT	BI-DIRECT	BI-DIRECT
REF. BOARD	NO	NO	NO	YES	YES
SOFTWARE	ON-LINE (DISK)	ON-LINE (DISK)	OFF-LINE (MAG CARD)	ON-LINE (MAG CARD)	ON-LINE (FLOPPY DISK)
IC TYPES	ALL	ALL	5-15V LOGIC	5-15V LOGIC	5-15V LOGIC
INPUT PWR	115V	115V	115V@3A	115V@7A	115V
STIMULUS	STORED PATTERN	STORED PATTERN	PSEUDO-RANDOM	PSEUDO-RANDOM	PSEUDO-RANDOM
RESPONSE	STORED PATTERN	STORED PATTERN	TRANS COUNT	TRANS COUNT OR R/D COMP	TRANS COUNT STORED PAT.
TYPE TEST	FUNC	FUNC	FUNC	FUNC	FUNC
TEST DEVEL. DOC.	SPEC SHEET & MOD LOGIC DIA	SPEC SHEET & MOD LOGIC DIA	SPEC SHEET & MOD LOGIC DIA	SPEC SHEET & MOD LOGIC DIA	
SELF TEST	YES	YES	YES	YES	YES
PHYS. DESC.	4 ea ½ BAYS	3 ea ½ BAYS	BENCH TOP	CONSOLE	CONSOLE
IN-CIRCUIT TEST	YES	YES	YES	YES	YES
DEVICE TEST	YES	YES	YES	YES	YES

SHEET 1 of 3

FIGURE B4

DIGITAL MODULE TESTERS (PRODUCTION)

	COMPUTER CONTROL				
	4050	4150	4250	4350	4450
CONNECTOR	64-383 pin	64-383 pin	32-192 pin	64-766 pin	32-384 pin
INTERFACE	FIXED	BI-DIRECT	FIXED	BI-DIRECT	BI-DIRECT
REF. BOARD	NO	NO	NO	NO	NO
SOFTWARE	OFF-LINE FLOP. DISK	ON-LINE FLOP. DISK	ON-LINE FLOP. DISK	ON-LINE FLOP. DISK	ON-LINE FLOP. DISK
IC TYPES	TTL	TTL OR CMOS	ALL	TTL OR CMOS	ALL
INPUT PWR.	115V@30A	115V@30A	115V@30A	115V@30A	115V@30A
STIMULUS	STORED PATTERN	STORED PATTERN	STORED PATTERN	STORED PATTERN	STORED PATTERN
RESPONSE	STORED PATTERN	STROED PATTERN	STORED PATTERN	STORED PATTERN	STORED PATTERN
TYPE TEST	FUNC.	FUNC.	FUNC.	FUNC.	FUNC.
TEST DEVEL. DOC.	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA
SELF TEST	YES	YES	YES	YES	YES
PHYS. DESC.	½ BAY	½ BAY	½ BAY	½ BAY	½ BAY
IN-CIRCUIT TEST	YES	YES	YES	YES	YES
DEVICE TEST	YES	YES	YES	YES	

SHEET 2 of 3

FIGURE B4 (CONT)

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DIGITAL MODULE TESTERS (PRODUCETION)

	DATA TEST 4800	5800	W/J ADATE	BENDIX HERBIE
CONNECTOR	256 pins	64-256 pins	128-512 pins	64-256 pin
INTERFACE	BI-DIRECT	BI-DIRECT	PROG.	FIXED
REF. BOARD	NO	YES	NO	NO
SOFTWARE	OFF-LINE	ON-LINE	ON-LINE FLOP. DISK	ON-LINE (PROM)
IC TYPES	5V LOGIC	ALL	ALL	5V LOGIC
INPUT POWER	115V	115V	115V	115V
STIMULUS	STORED PATTERN	2	STORED PATTERN	STORED PATTERN
RESPONSE	TRANS COUNT	TRANS COUNT STORED PATTERN	STORED PATTERN	STORED PATTERN
TYPE TEST	FUNC	FUNC	FUNC/PARA	FUNC
TEST DEVEL. DOC.	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA
SELF TEST	YES	YES	YES	YES
PHYS. DESC.	3 PIECE BENCH TOP	2 EA ½ BAY	1 BAY	BENCH TOP
IN-CIRCUIT TEST	YES	YES	YES	YES
DEVICE TEST	YES	YES	YES	YES

1 PROM, CASSETTE, PUNCH CARD
2 GREY CODE, PSEUDO-RANDOM, FIXED PATTERN, STORED PATTERN

SHEET 3 of 3

FIGURE B4 (CONT)

DIGITAL MODULE TESTERS (MAINTENANCE)

	TRENDAR 3010A	GEN RAD 1795	BENDIX HERBIE	SANDERS USM-392	W/J ADATE
CONNECTOR	128 pins	72-480 pins	64-256 pins	127-255 pins	128-511 pins
INTERFACE	BI-DIRECT	BI-DIRECT	FIXED	BI-DIRECT	PROG
REF. BOARD	NO	NO	NO	NO	NO
SOFTWARE	OFF-LINE (MAG. CARD)	ON-LINE (DISK)	ON-LINE (PROM)	OFF-LINE MAG. CASSETTE	ON-LINE FLOP. DISK
IC TYPES	5 - 15V LOGIC	ALL	5V LOGIC	TTL	ALL
INPUT POWER	115@3A	115V	115V@0.75A	115V25A	115V
STIMULUS	PSEUDO-RANDOM	STORED PATTERN	STORED PATTERN	STORED PATTERN	STORED PATTERN
RESPONSE	TRANS. COUNT	STORED PATTERN	STORED PATTERN	STORED PATTERN	STORED PATTERN
TYPE TEST	FUNC	FUNC	FUNC	FUNC	FUNC/PARA
TEST DEVEL.DOC	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA	SPEC SHT & MOD LOGIC DIA
SELF TEST	YES	YES	YES	YES	YES
PHYS. DESC.	BENCH TOP	2 ea ½ BAY	BENCH TOP	BENCH TOP	1 BAY
IN-CIRCUIT TEST	YES	YES	YES	YES	YES
DEVICE TEST	YES	YES	YES	YES	YES

FIGURE B5

APPENDIX B

ANNEX A

Siemens - Model 720

A. General Description

The model 720 digital IC tester is designed to perform functional and parametric tests on all digital circuit families. The tester utilizes a programming board to set all parametric values to be tested and a "known good" device to make all functional comparisons. Each IC device type requires its own individual programming board. Stimulus for functional testing is provided by a "grey code" converter.

Software test programs are not required for this tester.

B. Analysis

The model 720 digital tester is designed as a device (out-of-circuit) tester and cannot economically be converted to perform in-circuit test functions.

The "known good" device concept of testing always creates an interesting problem, how does one determine the "known good" device is actually good prior to the start of testing? The 720 does not have provisions to make this assessment.

The next problem encountered in the investigation was the requirement for a programming board for each type of IC tested. In a maintenance environment where a large variety of IC types are encountered the user would have to supply a large number of programming boards. The initial procurement costs and logictics costs associated with this test philosophy are very large.

As a result of these findings the model 720 was dropped from further consideration.

C. Characteristics

A.1. Digital IC Tester
2. Device or out-of-circuit tester
3. No in-circuit test capability

B. Interface - Model 721A - 16 pins, Model 724A, 24 pins

C. Power Supplies

D. Signal capability - ECL, HTL, CMDS, bidirectional, Grey code generator

E. Clocks

F. Type testing - parametric and functional (device compare)

G. Test Time

H. Storage Device - program board and "known good" device

I. Software devel. - N/A

J. Physical Disc

Other

1. No software required

2. Maint/diag.-manual

3. Training available

Comments

1. Each device type requires a program board

2. Functional tests require a "known good device".

3. Functional tests are made by comparing the outputs of the unit under test with the "known good device".

4. "known good device" cannot be verified on station.

Biomation - Sitek 2400

A. General Description

The model 2400 Digital IC Tester is a low cost functional tester servicing TTL, ECL, CMOS (5V), NMOS 5V), etc. The unit uses a psuedo-random gray code generator (4KHZ to 1.3 MHZ) to exercise a functional reference device and the UUT simultaneously. It then compares the output of each device to determine proper operation of the UUT.

The tester has over 140 controls on the front panel to program 14, 16, or 24 pin ICs. Each IC type tested requires an interface adapter containing interface wiring, test loads, and two IC test sockets for the 'functional reference device' and the UUT.

Test parameters are determined directly from the IC manufacturers data sheet or from a program library previously prepared by Biomation and supplied with the tester.

B. Analysis

The model 2400 requires considerable manual set-up time, two interface devices, and a "known good" reference device. The front panel controls require the operator to assign supply voltage, ground, clock, input,or output functions to each pin of the IC. He must also set the IC family type under test, tester operating mode, type of test and propagation delay time. To interface the UUT with the tester at least one general purpose device board is required for each 14, 16, and 24 pin package and load board. The load board must be changed to satisfy the load requirements of each device under test.

This tester requires considerable manual set-up, which increases the overall test time and allows human error to not only affect the test results but may also damage the UUT and reference device.

The Tester is capable of device or out-of-circuit testing only and contains no provision, nor can it be modified, to perform in-circuit test functions.

The unit does not provide a method of insuring the "known good" device is free of faults.

For the reasons stated above this unit was found to be unacceptable for this program and, therefore, was dropped from further consideration. (This is not to be construed to mean it does not have a useful place in other applications).

C. Characteristics

A.1. Digital IC tester
2. Out-of-circuit functional test capability
3. Cannot be adopted to in-circuit testing

B. Up to 24 pins using standard IC adapters

C. Power Supplies - 0 to +5.25V @ 300 MA,
Power Requirement - 115V @ 1.5A

D. Signal Capability - 5KHZ to 1.3 MHZ, combinational, sequential and preset

E. Clock - Internal @ 5KHZ to 1.3MHZ

F. Type Testing - pattern comparison with known good IC

G. Test time - 15 MSEC

H. Storage device - Test tables or manuals show tester front panel control settings

I. Software - update capability - N/A

J. Physical Description 17" x 17" x 6"

Software

1. N/A

Comments

This unit is primative in concept using manual setup of stimulus/response requirements of each IC pin and comparison check of IC under test with a "known good" unit. Manual intervention allows for man made errors each time a new IC type is tested and "known good" chip cannot be verified. But it is a very inexpensive way to test ICs. It is more suited to incoming inspection than as a maintenance tool. The tester is a "device tester" only and as such cannot perform in-circuit test functions.

Biomation - Model 3200A

A. General Description

The model 3200A digital IC tester automatically performed parametric and functional tests on most IC logic families in less that 150 msec per chip. All test parameters are set-up on a hardware 'program board' using 1% resistors. The program board also includes a functional reference device (known good IC) to generate output patterns for comparison with the out-put of the unit under test (UUT).

The tester performs 96 parametric tests in approximately 40 msec and up to 44,000 functional tests in approximately 110 msec at the highest clock frequency.

Functional Test -

A pseudo-random code is applied simultaneously to the functional reference device and the UUT; then their outputs are compared for similar logic levels.

Program Board -

A program board can be developed for each IC type to be tested or a universal board containing over 30 switches and a load board can be used for a variety of IC types. The latter requires operator adjustments whenever a different IC type is to be tested, thus adding the probability of operator error and faulty test results.

B. Analysis

The model 3200A provides parametric and functional testing of digital ICs by using dedicated programming boards. The board uses one percent resistors to set the value of each parameter tested and also contains a "known good" reference and functional test load resistors. One board may be used to test a number of IC types providing the test parameters, interface wiring, and load requirements do not change. The manufacturer can also provide a universal programming board containing over eighty switches and provision to connect an external load/reference test device board.

The dedicated programming board reduces the manual set up procedure and minimizes test documentation but can only be used for a very limited variety of devices. Therefore, the initial cost of a large variety of programming boards and the life-cycle logistic costs become prohibitive.

This unit does not have, nor can it be modified to perform, in-circuit test functions.

This model 3200A was found to be undesireable for the reasons stated above and, therefore, dropped from further consideration.

C. Characteristics

A.1. Digital IC tester
2. Out-of-circuit functional and parametric test capability
3. Cannot be adapted to in-circuit test

B. Up to 34 pin ICs using standard IC adapters

C. Power supplies - 0 to +20VDC, programmable with 1% resistors

D. Signal Capability - 20 to 400KHZ

E. Clock - internal 20 to 400KHZ

F. Type Testing - pattern comparison with a "known good" device for functional test, voltage comparison for parametric test

G. Test time - Para. 40ms, func. 110 ms

H. Storage Device - P/C board containing 1% resistors

I. Software Update - N/A

J. Physical Description - 17" x 17" x 6"

Software

1. N/A

Comments

1. This unit gives a more thorough test of ICs checking parametric limits as well as functional operation.

2. Each IC type requires an ID or program board where parameters are set using 1% resistors.

3. Functional Test requires a "known good" IC for comparison to suspect IC or IC under test.

4. Device is better suited to incoming inspection or production use than for maintenance.

5. Operator has less control and therefore integrity of test is much higher.

6. Basic cost of the unit within the Navy's ceiling price, but program boards escalate the life cycle cost rapidly, particularly when a large variety of devices are to be tested.

Testline - Model 2050 (AFIT)

A. General Description

The model 2050 is designed to test digital IC devices in both in-circuit and out-of-circuit configurations. Testline has patented a process by which they can independently test an IC while it is installed on an SRA, connected to other ICs, without regard to the logic states of any IC interfacing with the IC under test. It is the only true in-circuit IC tester on the market today.

Test software programs are developed on-station and stored on floppy disks.

Testline has over 500 standard IC test programs available for purchase. These programs are developed directly from the manufacturers truth tables and provide test logic for out-of-circuit testing, but they do not take into consideration special circuit configurations encountered in in-circuit testing which affect the truth table. For the latter, the user must modify the standard software to meet his particular test need. Software modification requirements are well within the capability of Navy maintenance technicians and can be accomplished on-line.

AFIT uses standard IC clips for in-circuit testing.

B. Analysis

The Testline 2050 (AFIT) is the only digital IC tester found during this study which is specifically designed to test ICs in both in-circuit and out-of-circuit configurations. AFIT operates on a pulsed power concept that treats IC in-circuit configurations as if they were in an out-of-circuit configuration. This significantly reduces the test hardware requirement and lowers software costs to a small percentage that required with other IC test systems.

The Naval Air Test Center (NATC) at Patuxent River evaluated AFIT for three months in 1976 and found the following:

1. Out-of-circuit Fault Detection
   Over 92% of the faults inserted were detected. The 8% undetected were traced to faulty truth tables supplied by the IC manufacturer, when the truth tables were corrected AFIT detected these faults.

2. In-circuit Fault Detection
   AFIT successfully detected all faults inserted on "known good" boards and located faults on known bad boards. Faults included bad ICs, solder shorts, and incorrect wiring.

3. The following defects and/or limitations were discovered.

   a. IC test clip had to be modified to accommodate high density boards.

   b. IC test clip would not penetrate conformal coating on P/C board.

   c. A mechanical means (scraping and/or grinding) had to be employed to remove conformal coating before testing could start. Due to the nature of conformal coating it was difficult to determine when the coating had been completely removed. This resulted in false fault indications and required further cleaning of the PC board.

   d. Standard IC truth tables must be analyzed for in-circuit wiring configuration to insure truth table validity. Where circuit wiring invalidates the standard input/output code the truth table must be modified and the test software modified (modified programs can be stored on floppy disk for future use).

   e. AFIT will only test 5 volt logic.

   f. Disk drive heads are not readily accessible for maintenance.

Testline was visited to determine whether the difficiencies noted in NATC's report had been corrected or if future corrective action was planned. The following response was received:

1. Disk head driver had been reoriented to make them more accessible.

2. IC clips would not be changed to solve the conformal coating penetration problem.

3. Suggested the Navy use the same technique to remove conformal coating as used by the FAA.

4. Power supply levels may be changed in the future to accommodate other logic families.

5. Program modification for in-circuit testing was not considered that difficult and should be handled on site by maintenance technicians.

As a result of these findings, AFIT with the Zero Blast-N-Peen unit was selected for evaluation.

C. Characteristics

A.1. IC Device tester
2. Device or out-of-circuit tester
3. In-circuit IC tester using patented pulse techniques

B. Interface - 14/16 pin and 24 and 32 pin adapters/clips

C. Power Supply - 5V @ 7 amps, 200 μs pulsed power, V_{cc} limit 1.2 A max (50 - 60 IC chips)
Power Requirement - 115 V

D. Signal Capability - 5 volt logic

E. Clock - 37Khz, internal

F. Type Testing - Static pattern compare and transition detection

G. Test Speed - 600 μsec/IC

H. Storage Device - Dual floppy disk

I. Software Development - on-line

J. Physical Description - 21" x 24" x 25" @ 134 pounds.

Other

1. Software developed on-line

2. Over 500 IC test programs available

3. Maint/Diag - Self test programs available

4. Training - Available

Comments

1. The Testline series of testers are the only IC testers available for in-circuit testing. They use a special pulsed power process which is patented by Testline.

2. The standard IC library available from Testline is comprised of test programs on devices used in out-of-circuit test configurations using the standard IC truth table. In many cases, each program has to be modified to accommodated circuit configuration such as NAND gates used as latches, inverters, etc., when used in in-circuit test configurations.

3. Can be used on TTL, DTL, CMOS(5V), low power Schottky ECL, etc.

4. ICs used in serial configurations must test a minimum of two ICs to determine the faulty IC. (IC output may be held to a zero level by the input of the next IC, there the following IC must be tested to insure its input is not faulty.)

5. IC truth table used to generate test programs for out-of-circuit testing while test programs generated for in-circuit testing must use the SRA logic diagram in addition to the standard truth table.

6. AFIT will test SSI and some MSI, but effective LSI testing is doubtful because of the short duration of the pulse. (even though it is advertized otherwise).

Teradyne - Model 133D

A. General Description

The model 133D was designed to support incoming inspection but does have the capability of testing digital IC devices in a maintenance environment.

Like many bench top testers, the Model 133D requires a programming card and a reference (known good) device to perform its test functions.

This device cannot be used to test ICs while installed on a board.

B. Analysis

The model 133D has many of the test aspects desired for a facility processing a large number, but limited variety, for IC devices. In the maintenance world just the opposite is encountered, a limited quantity of a large variety. The cost of logistics associated with the numerous programming cards and "known good" devices and its lack of in-circuit test capability makes this unit undesirable for NAEC's intended use and, therefore, was dropped from further consideration.

C. Characteristics

A.1. Digital Integrated Circuit Tester
2. Device or out-of-circuit tester
3. No in-circuit test capability

B. Interface - ZIF connector for 14, 16 & 24 pin DIPs

C. Power Supplies - 2.0 - 8.0 Vdc @ 0-250 MA

D. Signal Capability - TTL, DTL, HTL, HNIL, CMOS, and low power Schottky

E. Clocks -

F. Type testing - parametric and functional via known good device comparitor

G. Test Speed - 25 msec

H. Storage Device - None

I. Software Development - None

J. Physical Description - Bench Top

Other

1. Software - None
2. Maint/Diag. - Manual
3. Reliability - Extremely good
4. Training - Available

Comments

1. Each device tested requires a programming board.
2. Each family of devices requires a second programming board.
3. Device is easy to use.
4. Cost of programming boards and associated logistics is expensive for large variety of devices.
5. No method of verifying "known good" device.
6. Good production or incoming inspection tool.
7. Unit has no adjustments and requires no calibration.

Teradyne - Model J401

A. General Description

The model J401 IC test system will test TTL logic devices only. All programs are developed on-line through the use of a comprehensive key board containing 84 controls. The system was developed to test IC devices.

B. Analysis

The model J401 test TTL logic devices does not have an in-circuit test capability. The unit is far advanced over many IC logic testers but so is its price. For these reasons, the model J401 was dropped from further consideration.

C. Characteristics

A.1. Integrated Circuit Tester
2. No in-circuit test capability
3. Device or out-of-circuit tester

B. Interface -

C. Power Supplies -

D. Signal Capability - TTL logic

E. Clock -

F. Type Testing - dc parametric and static pattern comparison

G. Test Speeds

H. Storage Device - mag. tape cartridges

I. Software Development -

J. Physical Description -

Other

1. Software developed on station

2. Maint/Diag. - Available

3. Reliability - 10 year warranty

4. Training available

Comments

1. Data Logging capability
2. No programming language
3. Programmed directly from IC spec sheet
4. Good for large variety of devices (T^2L)
5. Too expensive
6. Single IC family application (T^2L Logic)

Macrodata - MD 104M

A. General Description

The model MD 104M was designed to test LSI including microprocessors. Its test capability and cost are much greater than required from the NAEC IC tester requirement.

B. Characteristics

A.1. Memory tester
2. Device tester

B. Interface - up to 10 test heads

C. Power Supplies

D. Signal Capability - memories, microprocessors, LSF, random logic

E. Clocks - 10 MHZ

F. Type testing - parametric and static, pattern comparison

F. Test Speed

H. Storage Device - paper tape, cartridge

I. Software Development - off-line

J. Physical Disc - 70 x 48 x 50, 1500 pounds (console)
- 30 x 72 x 30, 200 pounds (table)

Other

1. Software generated off-line

Comments

1. High speed unit making both parametric and functional test.

2. Too expensive.

3. Test capability far exceeds the requirements of this program.

Macrodate - MD-154

A. General Description

The model MD-154 was designed to test MOS/bipolar LSI devices at input/output speeds of up to 10 MHZ.

This unit has greater test capability than required for the NAEC IC tester requirement. It is also very expensive.

Too comprehensive for NAEC application.

Hewlett Packard - HP 5045A

A. General Description

The model HP 5045A is a bench top IC device tester designed to perform functional and parametric on a large variety of digital integrated circuits. It is one of the few IC testers containing a programmable interface capability and therefore, requires fewer and less complex interconnecting devices.

The tester contains a built-in thermal printer to permanently record all test values or just failure data or no data at the operators option.

Test software programs are developed by HP and supplied to the user in the form of magnetic strips approximately 12" long and 2½" wide.

B. Analysis

The model HP 5045A is designed for device testing only and cannot be modified to perform in-circuit test functions. This tester has two big advantages over most of the other IC testers.

1. It has a programmable interface.

2. It has on-line print out of failure parameters.

Software for the HP 5045A must be developed off-line at the HP software facility. This increases the maintenance facilities off-site liability and seriously delays testing of new devices and those requiring only minor software modifications. This was considered a major difficiency and therefore, not a satisfactory solution to the Navy's IC requirement.

C. Characteristics

A.1. Digital IC tester
2. No in-circuit test capability
3. Device or out-of-circuit test capability only.

B. Interface - 10 pins std., 24 pins optional

C. Power Supplies - $\pm$ 7.5V @ $\pm$200 MA
Power Requirements 115 V @ 2.2A

D. Signal Capability - ECL, CMPS, TTL, DTL, HTL, RTL, ROMs PROMs, & static RAMs; bidirectional universal pins.

E. Clocks

F. Type testing - parametric & static pattern compare

G. Test time -

H. Storage Device - magnetic strip

I. Software Development - Factory

J. Physical Description - 7.5 x 17 x 23 @ 86 pounds

Other

1. Software generated at HP software facility

2. Reliability -

3. Maint/Diag. - Program available

4. Training - Available

5. On-line magnetic strip duplicating capability

Comment

1. Hardware moderately priced.

2. Software could become expensive if unique programs are required.

3. Good approach to device testing.

Teradyne - Model J 149

A. General Description

The model J 149 is a linear device tester designed to test operational amplifiers and voltage regulators. The unit will perform up to 24 tests on a single device.

The device requires two programming boards, a family board and a device board to test a linear IC and a ROM module containing the necessary test software.

Software is developed at the factory.

B. Analysis

The model J 149 will not test linear ICs while connected in a circuit; it is a device tester only. Also, this unit requires two interface devices, one for each family of ICs and another for each IC type. At a maintenance facility where a large variety of ICs are supported the cost and logistics problems associated with interface devices become prohibitive. Therefore, this tester was dropped from further consideration.

C. Characteristics

A.1. Linear IC tester
2. Device or out-of-circuit tester

B. Interface - DIPs, flat pack (up to 24 pins)

C. Power Supplies 0 - 5Vdc

D. Signal Capability - operational amps and voltage regulators

E. Clocks - N/A

F. Type testing - parametric

G. Test speed - 1.0 sec.

H. Storage Device - ROM, RAM

I. Software Development - factory

J. Physical Disc - Bench type

Other

1. ROMs are programmed at the factory.

Comments

1. Provides 24 tests per device.

2. Temporary program modification can be accomplished on-line via keyboard.

3. Family of components requires program board (P/C) plus an individual device board, plus a ROM module.

4. Tester is more useable for small variety of test units.

5. Program boards and ROM module increase cost and logistic problems.

6. User is dependent on factory for ROM programs (no on-line programming capability).

Siemens - Model 735

A. General Description

The model 735 linear IC tester was designed to perform up to 14 tests on a variety of linear IC devices. The test parameters, sequences, etc. are determined by a device module and a performance (program) board. The latter sets up standard tests for device types (e.g. voltage regulator) while the former provides interface wiring and test parameters.

Software programs are not required.

B. Analysis

The model 735 is designed to test linear IC devices out-of-circuit and cannot be used for in-circuit testing. The tester requires two interface boards to test device module sets, device test parameters and wiring configuration while the performance board sets general requirements for a families of IC devices.

Each IC test device type tested requires a device module and each family requires a performance board. In a maintenance environment where a large variety of IC types are tested each day the number of interface devices required to support this test philosophy becomes prohibitive. Therefore, this tester was dropped from any further consideration.

C. Characteristics

A.1. Linear circuit tester
2. Device or out-of-circuit tester
3. No in-circuit test capability

B. Interface - determined by programming or performance board

C. Power Supplies -

D. Signal capability - DC and low freq. AC operational amplifiers, regulators, sense amplifiers, diff. amps, comparitors, custom linear circuits.

E. Clocks - N/A

F. Type testing - parametric

G. Test Time -

H. Storage Device - program board

I. Software development - N/A

J. Physical Description - Bench Top

Other

1. All programming accomplished on hardware - performance board
2. Reliability -
3. Maint/Diag - Manual
4. Training - Available
5. Test results can be recorded on standard peripheral devices.

Comments

1. All test values, switching, pin configurations, etc. are provided on performance boards via hardware implementation.
2. Tester automatically sequences tests, digitizes test results, and makes GO-NO/GO decision.

Biomation - Model 1440

A. General Description

The model 1440 is a device tester which automatically tests fourteen parameters on eleven different types of linear ICs. Test conditions for each IC are determined or programmed on a programming board where parameter values are set up using 1% or 0.05% resistors. All test sequences may be manually or automatically initiated with parameter values displayed for each test. The basic programming board (P/C) is purchased from Biomation with or without programming components or may be prepared by the user.

B. Analysis

This unit requires a program board to set-up all parameters to be tested and provide the necessary interface connections. Each linear IC family requires a separate program board. It does not have an in-circuit test capability.

C. Characteristics

A.1. Linear IC tester
2. Out-of curcuit tester
3. Cannot be used for in-circuit testing

B. Interface - Six to sixteen pins

C. Power Supplies - $\pm$ 50VDC @ 0 - 50 ma

D. Signal Capability - Analog - slow rate

E. Clock - N/A

F. Type Testing - Parametric

G. Test Time - 1.8 sec

H. Storage Device - Program board

I. Software update capability - N/A

J. Physical Description 17" x 17" x 8"

Comments

1. Tester has automatic test capability through the programmer board or manually through the manual programmer option.

2. Basic unit cost is within desired price range.

3. Programmer boards cause price to increase rapidly if a large variety of ICs are to be tested.

4. The absence of an in-circuit test capability and high life-cycle cost projections resulted in this tester being eliminated from any further consideration.

General Radio - Gen Rad 1730

A. General Description

The model 1730 is a linear circuit tester designed to test a variety of common linear ICs; operational amplifiers, comparitors, voltage followers, voltage regulators, etc. It can perform up to 18 tests on each linear circuit in less than 2 seconds.

An adapter board is required for each IC type to provide special circuitry and interface connections.

Programming is accomplished on the "programming board" containing 40 controls which must be set for each IC type.

All programs are run automatically with front panel readouts of all measurements available in the single step mode.

B. Analysis

The model 1730 provides rapid, precise testing of a large variety of linear IC devices. The unique hardware program board requirements have been minimized by using 40 controls to set up standard test conditions, unique test conditions are provided by an adapter board. Each IC type requires a unique adapter board. Where a large variety of IC's are tested (as at AIMD's) the initial cost and logistics cost would be large.

The model 1730 does not have an in-circuit test capability. As a result of these preliminary findings the model 1730 was dropped from any further consideration in the IC tester study.

C. Characteristics

A.1. Linear circuit tester
2. Out-of-circuit or device tester
3. No in-circuit test capability

B. Interface -

C. Power supplies -
Power Requirements - 115V@100 watts

D. Signal Capability - 17 individual analog tests

E. Clocks -

F. Type Testing - Analog

G. Test Time - 2.0 seconds

H. Storage Device - Mechanical prog. board

I. Software Device - N/A

J. Physical Description - 20' x 8' x 25', @55 pounds

Other

1. Software - N/A

2. Reliability -

3. Maint. - Manual

4. Training - Available

Comments

1. Linear units dropped from evaluation

Siemens - Model IT-200

A. General Description

The Model IT-200 digital/linear IC device tester is designed to perform functional and parametric tests.

Test software programs are developed off-line on a TTY (teletype) or at the factory and stored on PROMs.

B. Analysis

The Model IT-200 is a device tester designed to test digital and linear IC chips. This unit offers a great deal of versatility over most IC testers and does not require hardware program or device interface modules. The system will not test IC's mounted on circuit boards Software is developed directly from the IC manufacturers specification sheet.

The cost of the unit exceeds the ceiling set by NAEC. As a result of the testers price and since it is not able to test ICs in an in-circuit configuration, the unit was dropped from further consideration. (This is not to be construed to mean it could not be a cost effective approach to other test requirements.)

C. Characteristics

A.1. General purpose integrated circuit tester digital and analog
2. Device or out-of-circuit tester
3. No in-circuit test capability

B. Interface - 48 pins

C. Power Supplies 3 ea. ±30.48 @ 20 - 500 Ma
Power Requirements - 115V, 1Ø, 2.0A

D. Signal capability - bipolar, TTL, CMOS NMOS, PMOS, ECL, etc.

E. Clocks -

F. Type testing - parametric & static, pattern compare, test rate 100KHZ parametric and functional

G. Test Time -

H. Storage device - PROM (plug-in) or paper tape

I. Software Development - paper tape, 5 - 8 tape teleprinter or paper tape unit; PROM - off-line (factory)

J. Physical Description 20" x 18" x 22", @ 90 lbs.

Other

1. Software-paper tape programs (teleprinter) or PROMs (factory developed programs)
2. Reliability -
3. Maint/Diagnostic self test - available
4. Training - Available
5. Paper tape duplicating available
6. ROMs and RAMs testable when IT-200 is utilized with 901 tester. Test speeds up to 10MHZ maybe realized. Also test memory boards.

Comments

1. Good end to end tester
2. Off-line program development creates a problem
3. Tester is a moderate speed tester.
4. Both 200 and 901 configuration's require interface assemblies.
5. Analog test capability appears to be limited when compared to other testers.

Micro Systems - Model 500 Series

A. General Description

The Model 500 series tester is a bench top digital module tester using pseudo-random pattern generation and programmed stimuli/response test techniques. Even though pseudo-random pattern generation is used, the tester does not use a known good board for testing. Responses to the pseudo-random input are recorded for the module output and each mode on the module. Internal mode data is recoded on a schematic or listing and used during trouble shooting or fault location. An ATG software program, FLASH (Fault Location and Simulation Hybrid), is used to generate test patterns for stimulus and response where necessary. These features require a special software generation sub-system. Test software may be recorded on paper tape, magnetic tape cassette, disk, etc.

B. Analysis

Micro 500 Series is capable of testing ICs in both in-circuit and out-of-circuit configurations but was dropped from consideration because of off line test software development requirement.

C. Characteristics

A.1. Basically a module tester
2. Can be used to check ICs out-of-circuit.
3. In-circuit test capability available through module interface (stimulus), IC checked using multiple pin IC probe or single pin probe

B. Tester Interface - 223 edge connector pins; status display for all 223 pins

C. Supplies - 5V @ 6 amps

D. Signal Capability -

E. Clock - internal, external, sync, range

F. Type testing - static and pattern compare, dynamic transition count

G. Test Speed -

H. Storage Device - 1. Model 510 - PROM
2. Model 520 - Mag. tape cassette
3. Model 530 - punch tape
4. Model 540 - data link

I. No software update capability

J. Physical Description - 9" x 23" x 16" (portable unit)

Other

1. Test software - over 400 ICs
2. Software developed software station, via data link, or at MICRO
3. Maintenance -
4. Reliability -
5. Training - available

Computer Automation - Capable 4050

A. General Description

The Model 4050 is a computer controlled automatic logic curcuit tester designed to test and diagnose small to medium complexity (under 100 ICs) digital modules (TTL logic). Diagnostics are performed by using an IC clip and/or a probe.

Test programs can be developed on-line with the aid of a Model 4800, Logic Simulator System.

B. Analysis

The Model 4050 is capable of testing IC in both in-circuit and out-of-circuit configurations. However, this unit is a tester only and cannot be used to develop test software, nor can test software be modified for editing on this system.

As a result of the test software development deficiency this unit was dropped from the evaluation program.

C. Characteristics

A.1. Module tester, digital
2. Can be used to test ICs out-of-circuit
3. Can be used to test ICs in-circuit

B. Tester interface - 383 pins (expandable to 767)

C. Supplies - ±18V, Power Requirements-115VAC,60HZ, 30A

D. Signal Capability - TTL logic

E. Clock - internal @ 500 KHZ max.

F. Type testing - static, pattern comparison

G. Test Speed -

H. Storage Device - Floppy disk

I. No Software update capability

J. Physical Description - 36" x 26" x 35"

Other

1. Software generated off-line or with Model 4800
2. Maint/diagnostic programs available
3. Reliability - one year on site warranty
4. Training - available

Comments

1. Unit basically designed for module test but easily adapted to IC test in and out-of-circuit test functions over a broad range of IC types.
2. All stimulus and output response patterns contained on disk.
3. Minimum operator intervention - IC clip and guided probe.
4. System cost - Exceeded ceiling price.
5. In-circuit test accomplished by manipulating IC inputs at UUT interface and monitoring IC outputs at IC interface.

Computer Automation - Capable 4150

A. General Description

The Model 4150 is a computer controlled test and programming system designed to test, diagnose and develop software test programs for digital modules (TTL or CMOS logic) of low or medium complexity.

It utilized a probe and/or an IC clip to perform diagnostics down to the IC level.

B. Analysis

The Model 4150 can be used to develop test programs and ICs in both in-circuit and out-of-circuit configurations. It can be configured to test either TTL logic or CMOS Logic

The tester cost exceeds the ceiling for the application under consideration and was, therefore, dropped from further consideration.

C. Characteristics

A.1. Digital module tester
2. In-circuit IC tester
3. Out-of-circuit IC tester

B. Tester Interface 383 pins, expandable to 767

C. Power Supplies - depends on logic type

D. Signal capability - TTL or CMOS

E. Clock - 500KHZ

F. Type testing - static, pattern comparison

G. Test Speed -

H. Storage Device - floppy disk

I. Software update-on station

J. Physical Description 39" x 26" x 35" (cabinet) 31" x 26" x 34" (desk)

Other

1. Generated on station
2. Maint/diagnostics available
3. Reliability - one year on-site warranty
4. Training - available

Comments

1. Unit basically designed for module testing but has inherent IC test capability (in-circuit and out-of-circuit.)
2. All stimulus and response patterns generated on-line and stored on floppy disk.
3. Minimum operator intervention to attach IC clip and/or guided probe.
4. Cost of system with automatic test generator is over ceiling price
5. Limited analog capability can be added to the system.
6. In-circuit test capability provided by setting IC input logic via module interface and monitoring IC response at the IC interface via IC clip.

Computer Automation - Capable 4250

A. General Description

The model 4250 has basically the same test and software program development capabilities as the model 4150 except it can also test TTL, RTL, ECL, and CMOS logic.

B. Analysis

The model 4250 can test ICs in both in-circuit and out-of-circuit configurations and will test all logic families in the 0 to 18 volt range.

The system has more capability than the 4100 series but its unit cost exceeds the extablished program ceiling and, therefore, was dropped from further consideration.

C. Characteristics

A.1. Digital module tester
2. In-circuit IC tester
3. Out-of-circuit IC tester

B. Tester Interface - TTL, 64-384 pins, ALL 32-192 pins or a combination thereof.

C. Power supplies - $\pm$18V

D. Signal capability - ECL, CMOS, TTL, RTL, etc.

E. Clock - 500 KHZ

F. Type testing - static, pattern comparison

G. Test Speed -

H. Storage Device - 2 floppy disks and 5M BYTE moving head disk.

I. Software Development and update-on station

J. Physical Description - 39" x 56" x 34" (cabinet) 31" x 65" x 37" (desk)

Other

1. Software generated on station

2. Maint/diagnostic available

3. Reliability - one year on site warranty

4. Training - available

Comments

1. Unit basically designed for module testing but has interent IC in-circuit/out-of-circuit test capability.

2. All stimulus/response patterns generated on-line and stored on floppy disk.

3. Has floppy disk duplicating capability.

4. Cost exceeds program ceiling.

5. Limited analog capability.

6. In-circuit IC test capability provided by setting IC input logic via module interface and monitoring IC response at IC interface.

7. May be programmed for two different logic families simultaneously.

Computer Automation - Model 4350

A. General Description

The model 4350 is basically the model 4150 except for the addition of bidirectional logic lines. It will test TTL or CMOS logic.

B. Analysis

The model 4350 can test TTL or CMOS ICs in both in-circuit and out-of-circuit configurations but its cost exceeds the established program ceiling and was therefore, dropped from the evaluation program.

C. Characteristics

A.1. Digital Module Tester
2. In-circuit test capability
3. Out-of-circuit test capability

B. Tester interface - bidirectional
TTL - 767 pins, max.
CMOS - 384 pins, max.

C. Power Supplies - 18 volts programmable

D. Signal capability - CMOS, TTL, bidirectional

E. Clock - 500 KHZ

F. Type Testing - static, pattern comparison

G. Test Speed -

H. Storage device - two floppy disks and 5M BYTE moving head disk

I. Software development and update on station

J. Physical Description - 39" x 26" x 34" (cabinet)
31" x 65" x 37" (desk)

Other

1. Software generated on station

2. Maint/diagnostic available

3. Reliability - one year on-site warranty

4. Training - available

Comments

1. System basically designed for module testing but has inherent IC list capability for both in-circuit and out-of-circuit IC testing.

2. Has bidirectional test capabiility.

3. All stimulus/response patterns generated on line and stored on floppy disk or moving head disk.

4. Cost - exceeds program ceiling

5. Has option for limited analog capability.

6. In-circuit IC test capability provided by setting IC input logic via module interface and monitoring IC response at IC interface.

7. Has floppy disk duplicating capability.

Computer Automation - Model 4450

A. General Description

Same as 4350 except it includes ECL, CMOS, TFL, RTL, etc.

B. Analysis

System unit aquisition cost exceeds program ceiling and was therefore dropped from further consideration.

Teradyne - Model L125

A. General Description

The model L125 was designed to detect and diagnose manufacturing type faults on both analog and digital, printed circuit boards.

The system contains a large variety of analog and digital stimulus/ measurement services.

Test software generation appears to require a much higher skill level than is available in the Navy.

B. Analysis

The model L125 has more capability than is required for this program and its cost exceeds the established ceiling. This tester was dropped from further consideration.

C. Characteristics

A.1. Hybrid Module Tester
2. Suitable for in-circuit IC testing
3. Out of circuit testing

B. Interface -

C. Power Supplies - 0 to ±50Vdc, - 0 to 260Vac
Power Requirement - 115V, @ 40A

D. Signal Capability - DTL, TTL, ECL, MOS

E. Clock -

F. Type Testing -

G. Test Speeds -

H. Storage Device -

I. Software Development -

J. Physical Description - 3 bay console

[redacted]ent

Too large and too expensive

Data Test Corporation - Model 5800

A. General Description

The model 5800 is designed to test all currently used digital logic families. All testing and test programs development are accomplished on-line without the aid of peripheral equipment.

The tester used pseudo-random code, grey code, and fixed pattern stimulus.

The model 5800 contains a unique UUT connector assembly which can be rotated as much as 120° to allow probing of either side of UUT.

B. Analysis

This model 5800 provides a very comprehensive IC logic test capability but its cost far exceeds this programs ceiling and, therefore, was deleted from further consideration.

C. Characteristics

A.1. Digital Module Tester
2. In-circuit test capability
3. Out-of-circuit test capability

B. Tester Interface - 64 to 256 pins

C. Power supplies - 3 variable (programmable) 8 threshold supplies (prog) (0 - 30 Vdc)

D. Signal Capability - DTL, TTL, ECL, MECL, CTL, HTL, MOS, CMOS, etc.

E. Clock - 400 KHZ

F. Type testing - static, pattern compare and transition count

G. Test speeds - 200 - 400 KHZ

H. Storage Device - floppy disk

I. Software development on-line

J. Physical Description - Test head, 250 pounds, 37" x 23" x 39"; control console 275 pounds, 42" x 48" x 30"

Other

1. Developed on-line using symbolic test language
2. Maint/diagnostics - available
3. Reliability
4. Training - available

Comments

1. One of the most complete IC family test capabilities
2. No ATG
3. Good P/C board handling technique
4. Very expensive system

Fluk - Trendar 3040A

A. General Description

This unit was designed to test micro processors and LSI boards. Although it has the capability of testing ICs in-circuit or out-of-circuit configurations, it is much larger than is necessary to satisfy the NAEC IC Tester requirement. It is also more expensive than the budget will permit.

It uses "known good" board techniques to develop programs and stores test data on floppy disks.

Fluk - Trendar 3010A

A. General Description

The model 3010A is designed to test digital modules using pseudo-random pulse generation for UUT stimulus and transition counter at the UUT output and IC interfaces. The latter count is used for diagnostic fault isolation to the IC interfaces. The latter count is used for diagnostic fault isolation to the IC level.

Software test programs for the model 3010A are developed by applying a pseudo-random code to each input of a "known good" UUT and checking each internal node for proper truth table activity. Once the activity at each node has been verified the input pattern code for each UUT input and the number of UUT output transitions are recorded on a magnetic card which is the size of a standard credit card. (This program then becomes the end-to-end program for all suspect UUTs.) Diagnostic fault isolation is developed by running the end-to-end program and monitoring the transition activity of each internal node. This information is recorded on the schematic or a from-to lookup table.

B. Analysis

Using the model 3010A to satisfy the in-circuit test requirement of the Navy's IC tester program would not be satisfactory since all internal (IC) data are in the form of the total number of output transition counts occuring during the entire end-to-end test sequence also, the need for a from-to lookup table or schematic defeats the automatic test requirement and increases test time substantially.

The model 3010A has, therefore, been found to be an unacceptable candidate for the Navy's IC tester program.

C. Characteristics

A.1. Digital Module Tester
2. In-circuit IC test capability
3. Out-of-circuit maybe accomplished

B. Interface - 128 pins and one probe

C. Power Supplies - 5V @ 5A, 3-15V @ 1.0A, 15V & 100MA
Power Requirements - 115V @ 300 watts

D. Signal Capability - pseudo-random - over 700 patterns.
100 to 4MHZ bits/sec.

E. Clock - 4MHZ (max)

F. Type Testing - static transition count

G. Test speed - DFI several minutes (manual probing & table look-up are required to determine acceptable test values)

H. Storage Device - magnetic card (ABA size)

I. Software Development - on-line

J. Physical Description - 14" x 22" x 24" @ 55 pounds

Other

1. Software - on-line development and up-dating

2. The end-to-end program is developed by assigning set pattern groups to the input pins and determining the total number of corresponding output transitions.

Comments

1. Diagnostics are manual in nature and only capable of only evaluating one node at a time. Once the end-to-end test fails, manual probing is required to determine which output pins failed and finally which IC malfunctioned.

2. The DFI methodology is very time consumming and does not allow detection of propogation time malfunctions.

3. Node transitions must be determined from imperical data derived from testing a known good board (module) or many hours of engineering time must be spent to determine the number of transitions occuring at each node during the entire end-to-end test sequence.

4. The UUT is interfaced via a test adapter which will serve a family of boards sharing a common connector providing the power supply pins remain the same.

Fluk - Trendar 3020A

A. General Description

The Model 3020A is basically a comparative tester using pseudo-random code generation and a result requires a "known good" device to test a UUT. In addition it also has the transition count capability of the model 3010A.

Stimulus generator outputs are selected by a magnetic card (standard ABA credit card size) and when transition counting is employed the output transitions are also included on this card.

B. Analysis

The model 3020A requires a "known good" device to perform comparative test techniques. This technique eliminates the problems of the transition count tester but adds new problems which cannot be over looked.

1. Requires a "known good" device to perform all testing.

2. No provisions made to insure "known good" device has not failed since last test.

3. Storage of "known good" devices becomes a problem when a large variety of UUTs are to be supported.

The model 3020A was found to be unacceptable for the above reasons.

C. Characteristics

A.1. Digital module tester
2. In-circuit test capability
3. Out-of-circuit test maybe accomplished

B. Interface-128 module pins, 16 clip pins, 1 probe

C. Power Supplies - 5 volts

D. Signal Capability - pseudo-random, 700 patterns

E. Clock - 4MHZ max

F. Type Testing - diagnostic, logic compare and/or static transition count

G. Test Speed - DFI (manual node probing) is time consuming

H. Storage Device - magnetic card (ABA size)

I. Software Development-on-line

J. Physical Description - 46" x 66" x 32" 2,400 pounds

Other

1. Software - on-line development and up-dating

Comments

1. Diagnostics are achieved by comparing the UUT output to a "known good" SRA via a 16 pin clip or transition count probe.

2. System has a stop-on-failure advantage over 3010A.

3. Additional documentation required to determine fault path.

4. Diagnostics simpler and faster than 3010A.

5. The UUT is interfaced via a test adapter which will serve a family of boards sharing a common connector, providing the power supply pins remain the same.

General Radio - Gen. Rad. 1792A/B

A. General Description

The model 1792 was designed to test digital modules and LSI chips using several automatic test generator approaches: CAPS (Computer Aided Programming Software), AFI (Automatic Fault Isolation) computer guided tracking probe and smart probe. The system is capable of testing most logic families currently found in electronic hardware.

The ATG generates unique stimulus patterns for each UUT and the corresponding response patterns for an operational module. Diagnostics are generated by simulating faults at various circuit nodes and observing the resulting outputs at the UUT interface (fault library generation). Test software maybe generated on-line. Programs can also be generated by manual means.

B. Analysis

The model GR1792A/B will test IC modules and IC devices in both in-circuit and out-of-circuit configuration. For in-circuit testing IC input patterns are controlled from the modules normal input terminals and IC output are monitored with an IC clip at the IC interface.

This test was found to have more capability than required for the IC tester program and exceeded the price ceiling. Therefore, the unit was dropped from further consideration.

C. Characteristics

A.1 Digital Module & LSI Tester
2 In-Circuit IC test capability
3 Out-of-circuit IC test capability

B. Interface - module pins, IC clips, and a probe

C. Power Supplies ± 5V, ±20V, ±40V(programmable)

D. Signal Capability - bi-directional 0-12V, 0-28V remotely controlable.

E. Clock -

F. Type Testing - static, pattern comparison

G. Test Speed -

H. Storage Device - paper tape, single disk, dual disk

I. Software Development - on-line

J. Physical Disc 109" x 36" x 33" 2,000 pounds

Other

1. CAPS - Automatic test generator
2. O/S - can be changed on-line
3. Training - available
4. Reliability -
5. Main/diag. - Available

Comments

1. Too sophisticated and too expensive for NAEC planned use.

Macrodata - MD-107

A. General Description

The model MD-107 is a memory and digital system analyzer designed for production and engineering use. It is capable of testing IC devices, modules, and some electronic systems. The system is a large comprehensive digital test device using programmable pattern test techniques. The capabilities of this system far exceed the IC tester requirements as does its cost, therefore, this system was deleted from further consideration (this is not to be construed to mean the MD-107 may not be a satisfactory cost effective solution to other test requirements).

B. Analysis

Too large and expensive for NAEC application. Software development off-line with device tester.

Sanders - AN/USM-392A (V)

A. General Description

The AN/USM-392A(V) is a light weight portable digital module tester designed to that digital circuit card assemblies. Most diagnostics are performed through probing circuit nodes.

Software is developed off-line on a software development system.

B. Analysis

The AN/USM-392A(V) was initially considered because it is currently in Navy inventory and therefore would minimize some logistics problems. The tester is designed to test digital IC modules and has many of the features necessary to satisfy the Navy's IC tester requirement. But, it has one big disadvantage. All software must be developed off-line on another piece of equipment or at the manufacturers software facility, Any software modification or change no matter how slight must also be performed off-line.

This total dependency to off-line support restricts the test and maintenance versatility planned for IC tester sites, therefore, the AN/USM-392A(V) was deleted from further consideration.

C. Characteristics

A.1. Digital Module Tester
2. In-circuit IC tester
3. Capable of device or out of circuit testing.

B. Interface - 127 bi-directional pins

C. Power supplies - +5VDC
Power Requirement - 115V, 500 watts, 3Ø

D. Signal Capability - TTL logic

E. Clocks - 1MHZ max

F. Test Type - static, pattern comparison

G. Test Time -

H. Storage Device - Magnetic tape cassette

I. Software Development - off-line

J. Physical Description - 11" x 17" x 25", @ 50 pounds

Other

1. Software developed off-line
2. Reliability -
3. Maint/diag. -
4. Training - Available

Comments

1. Tester relatively expensive
2. Will only test TTL logic
3. Requires off-line test program generation
4. Requires special adapter for in-circuit testing
5. Excessive power input requirements

WATKINS JOHNSON - ADATE 1300 Series

A. General Description

The ADATE 1300 series digital assembly test equipment is designed to test all digital IC families and configurations currently in use in industry. The tester also has a programmable interface. Unit has test speeds up to 20MHZ.

Software is developed on-line using a high level english language (COLT) and stored on floppy disks.

The manufacturer will supply over 1,000 IC programs with the system at no additional cost.

B. Analysis

The ADATE 1300 digital assembly tester was one of the most comprehensive testers considered under this study program. It covers several test capabilities not available on other systems; propagation delay measurements, dynamic testing, pulse to pulse level evaluation, programmable interface, etc. ADATE systems are used by several Navy maintenance sites with a high level of success. Navy maintenance technicians develop test programs on-site for this unit in addition to using it as a test vehichle for a variety of digital P/C cards and digital IC chips.

The manufacturer provides over 1,000 IC software test programs with each station delivered. The units programmable function allow testing of all IC families currently in use.

However, within the frame work of this evaluation programs requirements, ADATE was dropped from further consideration because its cost exceeded the ceiling set by NAEC and its capabilities far exceed the needs of a pure IC tester. (This should not be construed to mean ADATE could not be a satisfactory cost effective solution to other test requirements).

C. Characteristics

A.1. Digital module/IC tester
2. In-circuit test capability
3. Device or out-of-circuit test capability

B. Interface - 112 bi-directional pins

C. Power Supplies - ± 28V programmable

AD-A084 961 NAVAL AIR ENGINEERING CENTER LAKEHURST NJ GROUND SUPP--ETC F/G 9/5
INTEGRATED CIRCUIT TESTER EVALUATION STUDY.(U)
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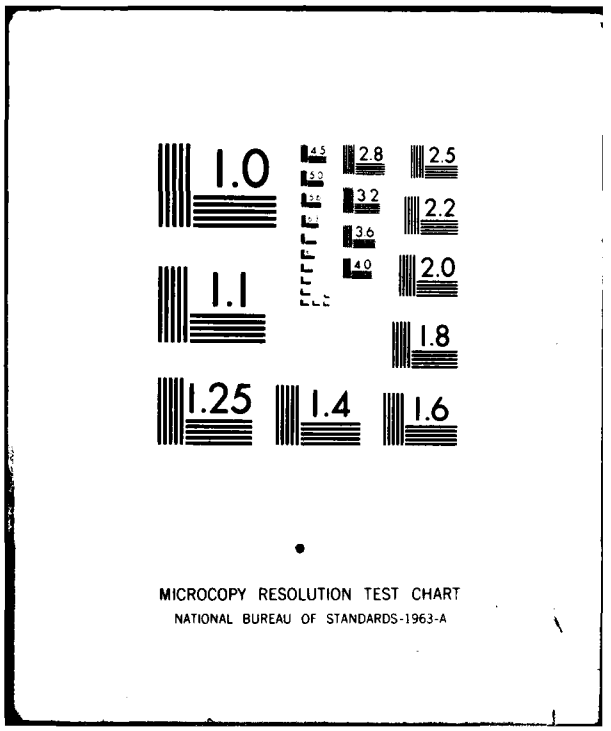
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

D. Signal Capability - TTL, DTL, ECL, CMOS, NMOS, PMOS, etc.

E. Clock - 20 MHZ max

F. Type testing - dynamic pattern compare - parametric (voltage only, pulse & DC level)

G. Test time - milleseconds at board level

H. Storage Device - Dual floppy disc

I. Software Development - on-line

J. Physical Description - 23" x 36" x 68", @ 80 pounds

Other

1. On-line software development

2. Reliability -

3. Maint/diag. progs. provided

4. Training-available

5. Over 1,000 IC test programs available.

Comments

1. Programmable power supplies and signal levels accommodate a large variety of IC families.

2. Tester relatively expensive for this application.

3. Presently programmed and used at Navy installations.

Bendix - Model 13A9070 (HERBIE)

A. General Description

The model 13A9070A is a small compact tester designed to test digital I.C. modules and devices.

Software test programs are developed on a TTY and the programs are transferred to PROMs using a PRO-LOG Model 900 or can be stored on an optional magnetic tape cassette.

Software test programs can also be generated on a Bendix developed CAFIG automatic test generator.

B. Characteristics

A.1. Digital Module Tester
2. In-circuit test capability
3. Device or out-of-circuit test capability

B. Interface - 256 pins

C. Power Supplies - 5V @ 4-5 amps
Power Requirements - 115V @ 750ma

D. Signal Capability - TTL, DTL, CMOS, etc. @ 2KC, tri-level

E. Clock - 2KC

F. Type Testing - static, fault library pattern compare

G. Test Time - 1Msec.

H. Storage Device - PROMs, mag tape, cassette

I. Software Development - on-line, programmer, with teletype and PRO-LOG

J. Physical Description - 19" x 19" x 8", @ 30 pounds

Other

1. PROM resident software, mag. tape cassette option

2. Maint/Diag. - auto to SRA and special programs to the component

3. MTBF - 3000 Hrs.

Comments

1. Uses the standard IC clips (do not penetrate conformal coating).

2. Will provide needlepoint IC clips to penetrate coating and DVM to verify contact with IC pins.

3. Power supplies manually adjustable for other logic families.

C. Analysis

The HERBIE IC module tester was originally designed to test IC modules with a 256 pin interface but the tester also has the ability to test IC devices alone (out-of-circuit) and while installed on P/C boards (in-circuit) with the aid of an IC clip. In-circuit testing is accomplished by manipulating the IC input through the P/C board interface and monitoring the IC response with an IC clip. Input test patterns can be generated manually or with the aid of CAFIG or other suitable automatic test generators.

Bendix was very cooperative in helping solve the conformal coating problem. They agreed to:

1. Provide an IC clip which used sharp, piercing pins to penetrate the conformal coating. (They would be similar to the phono tip needle points used for many years to solve this problem.)

2. Provide a continuity test of each active IC pin to insure contact prior to initiation of the in-circuit functional test of an IC.

Bendix was on a very tight development/production schedule but gave assurance they could and would meet the Navy's test/evaluation schedule.

The only negative aspect of the HERBIE system was two other devices were necessary for field use; a TTY and a PRO-LOG programmer. The TTY is normally found at all Navy maintenance sites and the PROM programmer is a small, inexpensive (> $1,800) device. This added to the cost of HERBIE (under $10,000) is the most cost effective hardware solution found during the study.

As a result HERBIE was chosen as the second tester to be evaluated.

Due to Bendix production problems, this tester was eliminated from further consideration.

Data Test Corporation - Model 4800

A. General Description

The model 4800 provides test capability for most IC families. Test program development must be performed off-line.

B. Analysis

The model 4800 does not have an on-line test program development capability. This is accomplished on another piece of hardware. The combined costs of these two units exceed the ceiling for this program and, therefore, the model 4800 was dropped from further consideration.

C. Characteristics

A.1. Digital Module Tester
2. In-circuit test capability available
3. Out-of-circuit test capability

B. Tester interface - up to 256 pins

C. Power Supplies - 5V $\pm$ 0.25V @ 3A
Power Requirement - 115Vac @ 400 watts

D. Signal Capability - DTL, TTL, MOS, CMOS, ECL, Etc.

E. Clock - Internal 2MHZ MAX, Ext. 5MHZ MAX

F. Type Testing - static, pattern comparison and transition counting

G. Test Speed - 2 - 34 seconds

H. Storage Device - PROM, EROM, or magnetic tape cassette

I. Software Development - on separate device.

J. Physical Description - 39½" x 60" x 34", @376 pounds

Other

1. Software generated on 8080 for PROM & EROM, 8010 for cassette

2. Maint/Diagnostics - Available

3. Reliability -

4. Training - Available

Comments

1. In-circuit testing can be implemented but with some difficulty since IC clip is not available with system (they use a single point probe, therefore, the ID would have to be modified to accommodate an IC clip.

2. Programs must be generated on separate software development system.

3. System components could be configured in smaller area/or for special installations.

General Radio - Gen. Rad. - 1795

A. General Description

The model 1795 Logic Circuit Test System was primarily designed as a maintenance tool and used L/TM (Learn/Test Mode) to generate test programs. A "known good" board is used to develop the end-to-end test software and all internal nodal data to be used in diagnostics. CAPS, guided probe, smart probe, etc. are available as options. The test engineer or programmer must determine the input patterns necessary to operate each circuit node and insure stuck at "0"s or stuck at "I"s are propogated to the UUT interface during the test sequence.

B. Analysis

The GR 1795 provides a functional test capability designed for maintenance facilities. Software is developed on-line using a "known good" IC module; once the software package is validated the program is stored on a diskette and there is no further need for the "known good" module. The tester can test ICs in in-circuit and out-of-circuit configurations.

The limiting aspects of this system are its size and cost which both exceed the program ceiling. Therefore, the tester was dropped from further consideration. (This is not to be construed to mean the tester would not be a cost effective solution to other test requirements.)

C. Characteristics

A.1. Digital module tester
2. In-circuit test capability
3. Out-of-circuit test capability

B. Interface - Module - 72 pins, expandable to 480 pins; probe, IC Clip - 16 pins

C. Power Supplies - 5V @10A, fixed
Power Requirement - 115V @ 40A

D. Signal capability - bi-directional, 1-12V logic levels

E. Clocks -

F. Type Testing - static, pattern comparison

G. Test speed -

H. Storage device - floppy disk

I. Software development - "known good" board, on-line; CAPS, off-line

J. Physical Description - 44" x 36" x 39"

Software

1. Developed on-line using "known good" UUT, with results stored on floppy disk.

2. Disk/memory overlap for long programs.

3. Training available -

4. Reliability -

5. Maint/diag. - program available.

6. Paper tape available

Comments

1. Known good unit required to develop programs on-line.

2. Probing method can be required to reduce large ambiguity groups.

3. System is expensive.

APPENDIX C

NAEC'S AFIT EVALUATION PLAN

NAEC's AFIT EVALUATION PLAN

The TESTLINE AUTOMATIC FAULT ISOLATION TESTER (AFIT) will be evaluated in the following ways:

A. Program Generation:

(1) Navy personnel will attend a one week training course at the manufacturer's facility, at which time it is expected that they will acquire the skills necessary to program the tester and to be able to operate it. At the completion of this training the technicians will be assigned numerous SRA's to program to enable the AFIT to demonstrate its ability to test circuit boards and isolate failed components and also to demonstrate that the training course was effective in imparting supportive skills to its students.

(2) A log will be maintained that will record an identification of the SRA's programmed, along with the number and type of IC's mounted on it (Fig. C1). The programming time will also be noted to assist in calculating Life Cycle Costs relative to testing and repairing SRA's with and without the utilization of the IC tester. The effectiveness of the Navy generated programs to correctly identify failed components will also be evaluated.

B. SRA Tests:

(1) A record will be kept to document the results of all SRA's tested on the AFIT (Fig. C2). This log will contain test times, identification of the failed IC, if determined, results of out-of-circuit testing of the suspected failed component and results of re-testing the repaired circuit board on an Automatic Tester (HATS or other) or by replacing it in its next higher assembly to determine that it is now operating properly.

(2) A record, for comparison purposes, will be kept of the SRA's that proceed through the repair cycle that are not tested by the AFIT, but are repaired by convential means (Fig. C3). Test time, repair time, and wait-time (i.e. time spent waiting for the required spare-parts to be received, if not immediately available).

C. Tester Reliability & Maintainability:

A log will be kept of the malfunctions of the AFIT along with its probable cause and corrective action taken (Fig. C4). The record will enable NAEC to determine the maintainability problems that may be expected when using the tester. A ratio of downtime to operational time will be kept to establish a basis of determining the mean-time between failures of the equipment under evaluation.

D. Component Spares Testing:

Since the AFIT has the capability to test IC's out-of-circuit, an effort will be made to test the spare stock of IC's. This will enable a determination to be made of their percentage of new IC's received from the

vendor, that are defective and are the cause of both a loss of time and money when used to replace faulty components. Although this effort is not directly related to the main evaluation task, it is felt that the information gathered during this effort will be extremely valuable in suggesting improvements or changes in testing procedures (see Fig. C5).

E. Program Analysis:

At the completion of the AIMD evaluation a complete analysis will be prepared for all aspects of the IC tester program. This information will constitute a segment of a larger NAEC study report to recommend a method for testing IC's both in-circuit and out-of-circuit.

PROGRAM LOG

FIGURE C1

Date	SRA No.	TTL IC No.	DTL IC No.	No. TTL Std Prog.	No. DTL Std Prog.	Total SRA Prog. Time	Remarks	Prog. Name

FIGURE C2 ATE/AFIT TEST LOG

Date 1	SRA No. 2	Ser.No. 3	No. of IC's 4	ATE Test Time 5	No. of Fail.Tests 6	Ambiguity No/Fail 7	IC Tester Test Time 8	Des. Fail.IC 9	IC Test out of Ckt 10	Repl IC Time 11	IC Retest Time 12	Fail/ Pass *13	Oper. Name 14	Remarks 15

*If fail, repeat items 8 thru 13.

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FIGURE C3 ATE/IC WITHOUT AFIT

Date 1	SRA No. 2	Ser. No. 3	No. of IC's 4	ATE Test Time 5	No. of Fail Tests 6	Ambiguity Group 7	IC Repl Time 8	Retest Time 9	Fail/ Pass *10	Oper. Name 11	Remarks 12

*If fail, repeat items 6 thru 10

FIGURE C4

OPERATION/MAINTENANCE LOG

Date	Elapsed Time	Malfunction	Corrective Action	Time To Repair	Oper. Name

COMPONENT TEST LOG

DATE	PART NO.	MANUFACTURER	NO. TESTED	NO. FAILED	OPER	REMARKS

FIGURE C5